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Research and Development Technical Report
DELET-TR-78-2935-F

MILITARY ADAPTATION OF COMMERCIAL ITEM (MACI) PROGRAM ON ELECTRICALLY ALTERABLE READ ONLY MEMORY

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October 1980

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Comparison of MNOS Device performance, device type selection, development of screening tests, and test plan.

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

1. INTRODUCTION

The MACI-EAROM program and other similar MACI programs address the very significant dilemma faced by the U.S. military with regards to availability of semiconductor integrated circuits (ICs) of LSI level and above. In the early years of IC development, the government/military work was the driving force behind the semiconductor industry. This was reflected in the fact that a majority of ICs were developed for military range operation after which most devices filtered down to commercial use. In more recent times this picture has reversed completely. Most ICs are currently being developed for commercial range operation and optimized for similar applications with regards to organization and I/O interface. These devices generally do not consider extended range operation in their design. Currently, it appears that the military can hardly get the attention of the semiconductor industry, let alone command the direction of its development.

It has been found however, that many ICs developed for commercial use will, in fact, operate over the ranges desired by the military. The MACI (Military Adaptation of a Commerical Item) programs developed by the Army at ERADCOM recognized this problem and are designed to examine promising commercial devices for use in military systems. By characterizing and analyzing the device performance at extended operating ranges, each IC can then be specified for use in military systems. This approach not only addresses the availability of devices but allows the military to capitalize on commercial development efforts. The multisource position of most commercial devices reduces logistics problems and doesn't require that the military be the sole support of semiconductor production facilities. This approach (MACI) represents an innovative and significant change to solving military logistics and technology development problems.

The other alternative possible to the military is the use of captive facilities totally supported from defense and government funding. This would be used to design and develop devices for special military requirements. The prime disadvantages of that approach is the high cost and lack of ability to capitalize on industrywide advancements.

Some of the contributions that can be credited to this program are:

- Identification of defense industry needs with regard to non-volatile memories.
- Collection and organization of MNOS industry inspection procedures and comparison to MIL-STDS.

- Explanation of MNOS memory test techniques.
- Exhibition of comparative device performance on a wide range of parameters.
- Explanation and demonstration of threshold measuring techniques and demonstration of their use in read-disturb, static retention and endurance prediction.
- Development of a nondestructive accelerated endurance prediction method for use in 100 percent screening of MNOS memories.
- Presentation of a significant amount of data with regards to performance in radiation environments of commercially available devices.
- Development of a rigorous test pattern designed for use in testing EAROMs and WAROMs (asymetric slant).
- Development of a prospective slash sheet to specify and test ER3400/NCR2451 type devices for military use.

Other contributions to the MNOS device technology knowledge can be found in the three Interim Reports.

It should be reiterated here that due to the financial limits of the program, the total test data base is relatively narrow. Data on the nonselected devices was taken from, at most, thirty devices from a single lot. Even the selected devices (ER3400/NCR2451) had a maximum of several hundred devices, representing a maximum of three lots. Therefore, the results may reflect the peculiarities of those lots rather than the general device characteristics. In order to gain confidence in the performance characteristics of these devices, current on-going characterizations should be instituted to insure device circuit designs or processes do not change in a way significant to planned operation. While the tests were honestly performed and measurements accurately taken, responsibility for use of the results is left to confirmation by potential users.

2. SCOPE OF FINAL REPORT

The scope of the MACI-EAROM Final Report is as follows:

- Reviews the concepts and goals of the MACI EAROM program.
- Reviews the results of the government/defense industry surveys.
- Reviews updates of the status of the MNOS memory industry and devices.

- Review of the selection criteria used to pick the final candidate device type.
- Reviews the results of the preselection phase tests and characterizations.
- Reviews the selection of the final device type and development of the test plan.
- Reviews the screening test results.
- Shows the development of the accelerated tests for time related parameters and the impact they are predicted to have on test cost and increased confidence in use of MNOS.
- Identifies the proposed slash sheet for the ER3400/NCR2451 parts.
- Presents new radiation test data.
- Presents new applications data.
- Presents recommendations for new studies in related technology areas.

3. PROGRAM PLAN

The MACI Program Plan, Figure 3-1, shows that the Final Phase primarily consists of delivery of required items such as:

- 50 Screened devices
- Final Test Plan
- Proposed Slash Sheet
- Last Data Items (Monthly Reports).

An additional item is the remaining End of Contract demonstration which will take place on October 7, 1980 at ERADCOM. Upon completion of this meeting all contracted work for the MACIEAROM will have been completed.

4. REVIEW OF INDUSTRY SURVEY AND PRESELECTION PHASE OF PROGRAM

4.1 Military/Defense Industry Device Survey

The purpose of this survey was to determine optimum device characteristics as used or desired by the defense industry for non-volatile, electrically alterable, read mostly memories. This data was then analyzed and the results used as part of the selection

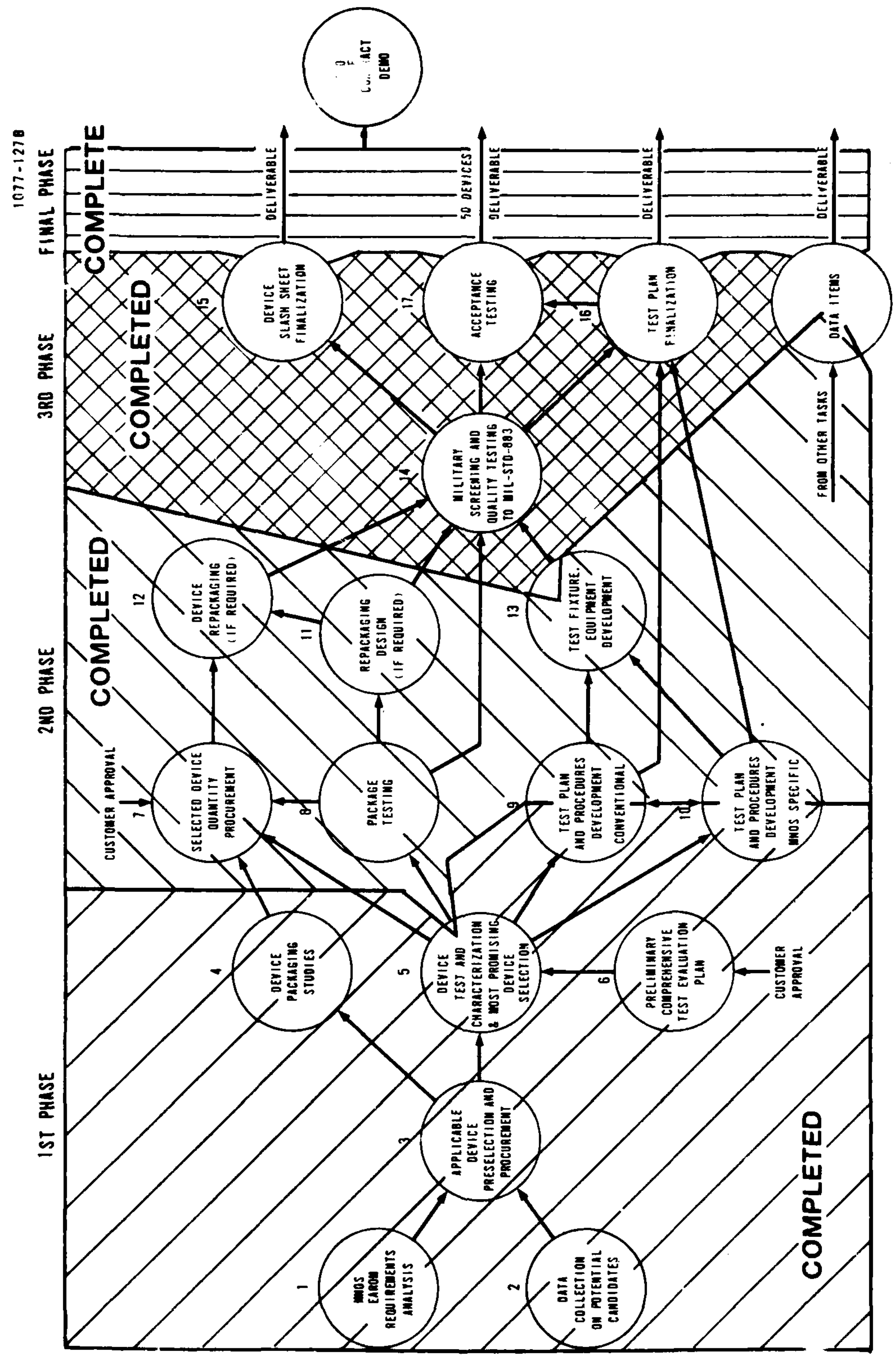


FIGURE 3-1. MACI-MNOS EAROM PROGRAM

criteria to determine which available EAROM device type would be optimum for use as the end device in the MACI program. The data was also used to develop the test and characterization plan to be performed on each device type.

One of the first questions that arose in trying to pick the best device type is: where are EAROMs used? Figure 4-1 shows the results of the survey. These results indicate EAROMs/WAROMs are desired for use in the mini/microcomputer applications and in places where special environments or higher reliability is desired. The lack of interest in fast random access applications (i.e., character generators, microcode memory) may reflect the current relatively slow speed status of the device technology rather than the actual desired use.

After determining where the devices were to be used, the reasons for selecting a part for those applications were explored. Figure 4-2 shows the relative importance given to several characteristics of MNOS devices. The usual parameters significant in selecting memory devices in general show up as the prime criteria for picking EAROM devices. These are:

- High density - large number of bits per chip
- Low power
- Low cost
- Fast access.

The obvious characteristics of nonvolatility tied in with an electrical erase and write capability weighs heavily in this choice. Two characteristics which did not attract initial attention in the preliminary survey and which have increased in importance in the intervening time are the ability to be packaged in hybrid configurations and the radiation resistance characteristics. With increased emphasis on replacing expensive magnetic memories in radiation hardened roles with less bulky lower cost semiconductor systems, a renewed look at this criteria was indicated. A drive is on to replace all mechanically rotational systems with more reliable, easier packaged nonvolatile systems that will operate in more stringent environments. In order to obtain densities near those possible with discs, drums or tapes, hybrid packaging techniques are necessary in employing MNOS devices.

Other survey results showed that high capacity devices with a byte organization would be more desirable with a four-bit (nibble) I/O trailing close behind. The most desired packaging was in

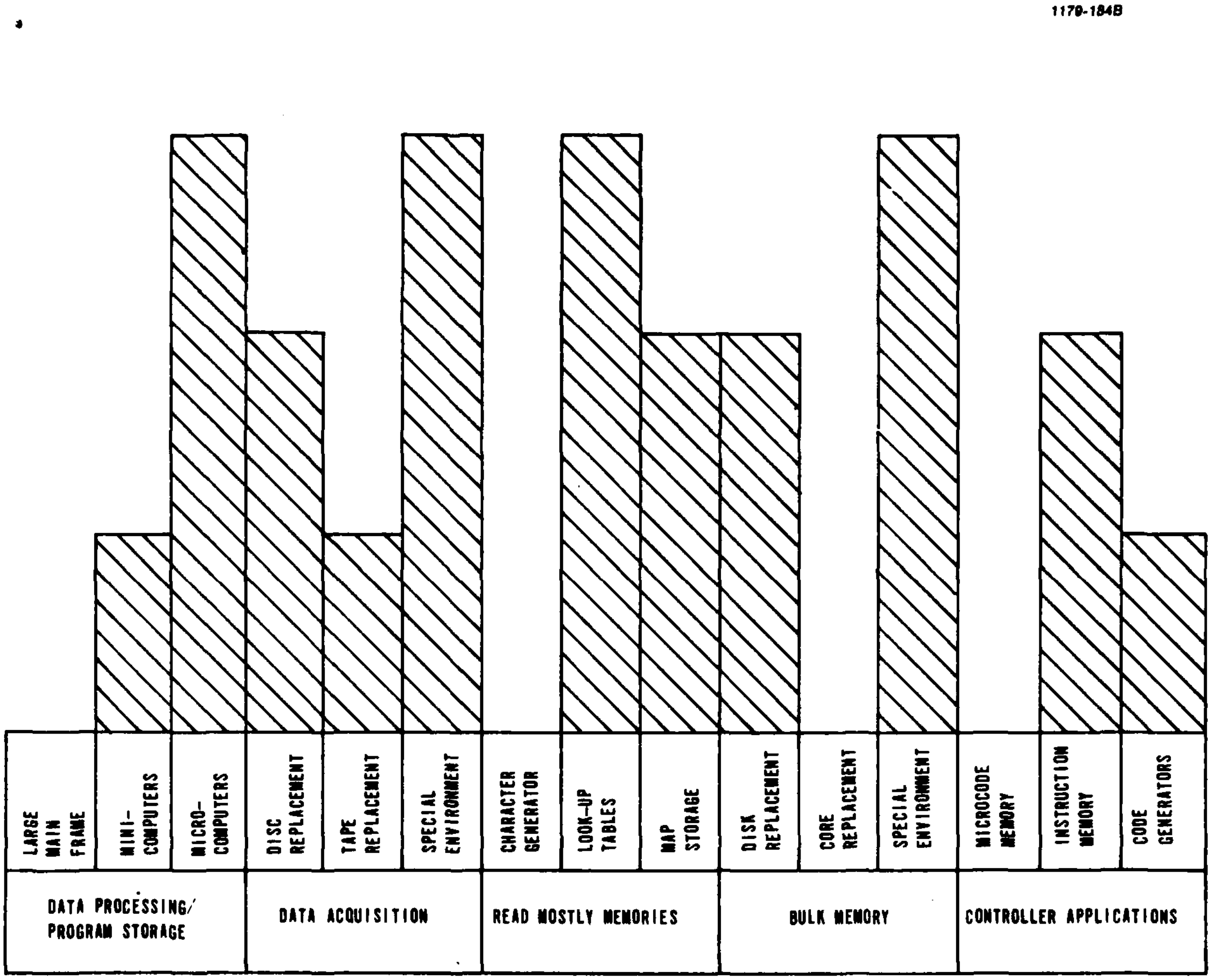


FIGURE 4-1. MNOS APPLICATIONS

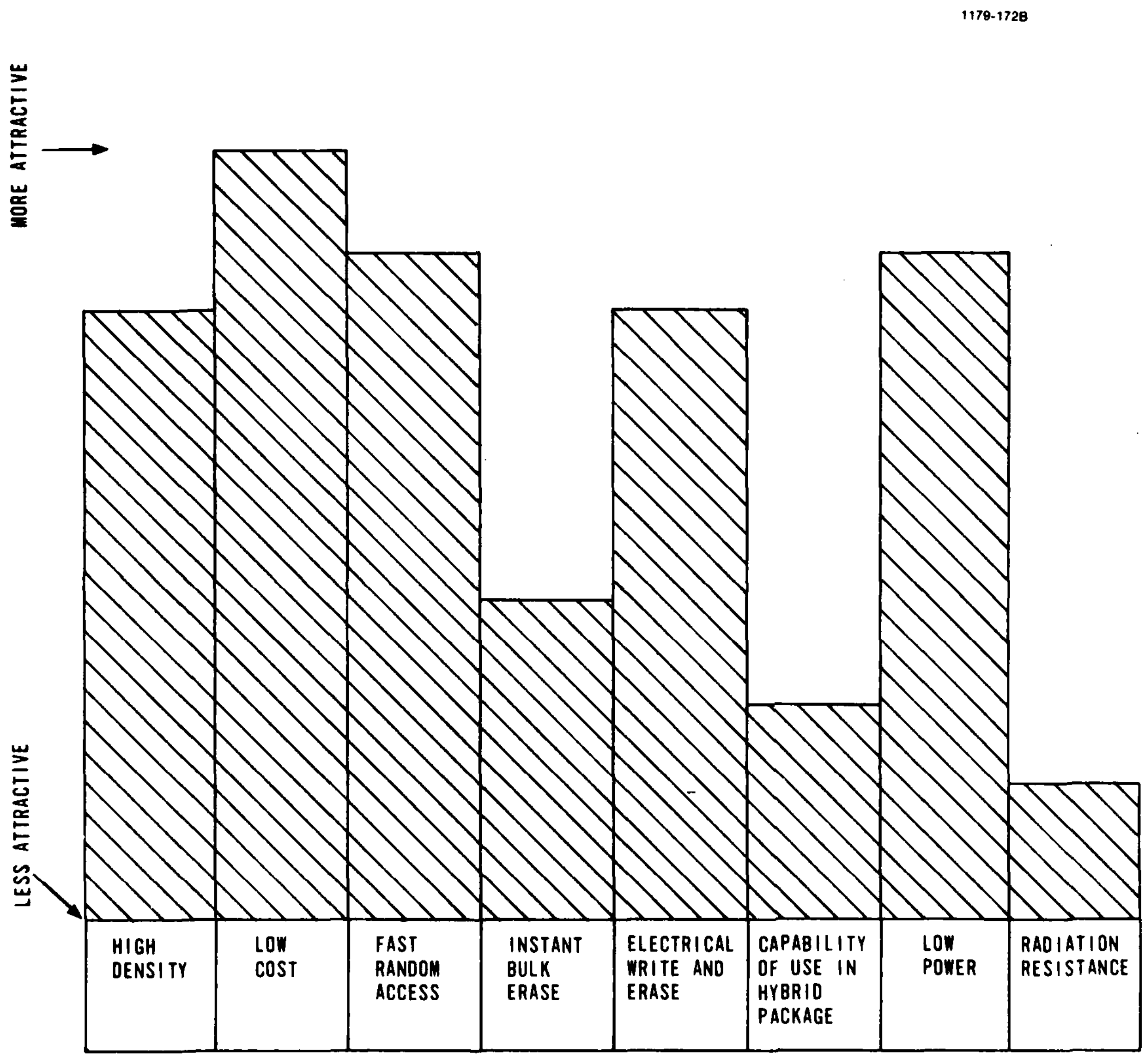


FIGURE 4-2. MOST ATTRACTIVE MNOS CHARACTERISTICS

standard width DIPs (16 pin, 18 pin, etc.) with 24 pin arrangements acceptable. Flat pack packaging was of some interest also, with the lower pin counts favored. A minimum temperature range of -55°C to +85°C was needed with full military range desirable. Other characteristics considered desirable were:

- Threshold testability
- Single chip select
- TTL or CMOS I/O compatibility
- Single standard power supply or a minimum number of supplies
- NDRO (nondestructive readout)
- Word erasability
- Memory status output.

Other characteristics considered acceptable but less desirable were: bulk erasability, a high voltage clock (+5V=Voh, -23V=VOL), and triple power supply voltage.

Figure 4-3 illustrates some of the most important characteristics of MNOS memories. These are generally the least understood parameters and the hardest to predict or screen test. It can be seen from the survey results that there are thresholds of acceptance in all three time-related parameters of retention, read disturb retention, and endurance. With regards to "static" retention, six months appears to be a minimum acceptable level, with most preferring in excess of one year. Read disturb retention (i.e., number of times a single address can be read before the data is disturbed) must reach limits in excess of 10^9 reads to be acceptable. Endurance (i.e., number of erase/write cycles performed on a particular address before device "wears out") levels must reach a minimum of 10^5 E/W cycles to be acceptable to most users, with 10^{10} E/W cycles desired.

The cost response is as expected: the lower the cost per bit the more desirable the response. The maximum cost where good approval is shown is at 0.25¢/bit.

4.2 Selection Criteria

The criteria that was used to select the optimum device was developed from survey data and MACI requirements. Table 4-1 shows the minimum selection criteria developed from this analysis.

TABLE 4-1. MINIMUM SELECTION CRITERIA

Parameter Classification	Selection Parameter	Optimum Value From Survey	Minimum/Maximum Value for Significant Use	Comments
1. Device Organization	a. Number of bits	16K	2K	8K and 4K bit devices in wide use. MACI Spec ≧-1K bits/device. No. 8 bit/word devices available (pins/package = lim).
	b. Number of Bits/word	8	4	
	c. Number of chip selects	2	1	Up to 4 CS is desirable.
	d. Programmable chip selects	1	0	Desirable but unimportant.
	e. Number of power supply voltages	1 +5 Vdc	3 +5 Vdc -12V and -30V	Lower number voltages desirable. Standard voltages important (i.e., +5V, ±15V, ±12V, etc.)
2. Performance characteristics	a. Access Time	<500 ns	Undefined	Times access ≦1 μs desirable. MACI requires ≦2 μs.
	b. Temperature range of operation	-55°C to +125°C	-55°C to +85°C	
	c. Data Retention (Static)	1 yr (10 yrs desirable	6 mos, 1 yr specified	Some use down to 24 hours MACI Spec 1 yr.
	d. Read Disturb retention (No. of Read Cycles before loss of data)	10^{12} cycles	10^{9} cycles	Some use down to 10^{6} cycles.

TABLE 4-1. MINIMUM SELECTION CRITERIA (Continued)

Parameter Classification	Selection Parameter	Optimum Value From Survey	Minimum/Maximum Value for Significant Use	Comments
2. Performance characteristics	e. Endurance (No. of write/erase cycles before device wearout)	10^{10} E/W cycles/bit	10^5 E/W cycles/bit	Some use down to 10^3 cycles. Some systems require 10^6 E/W cycles. Desired MACI Level $\geq 10^6$ E/W.
3. Packaging	a. Package type	Dual-in-ceramic	Flat pack Gold Kovar	Flat pack unacceptable in some MIL Appl.
	b. Number pins	16	24	
4. Power Consumption	a. Active Power (no standby)	100 mw/4K bit/dev	200 mw/4K bit dev	NOTE: Power Consumption was considered significant to device use in Military Systems.
	b. Active + stand-by power	100 mw/4K dev Active OW stand-by	300 mw/4K dev Active 50 mw stand-by	
5. Cost	a. Price/Bit	≤0.25¢/bit	≤2.0¢/bit	
6. Write/Erase Conditions	a. Write/Erase voltages	+5V preferred	Single Write/Erase voltage ±0±30V	MACI requires ≤±35V.
	b. Write/Erase time	≤100 μs preferred	≤50 ms Write ≤500 ms Erase	Tied to retention of ≥1 yr required or ≥3 yr desired.

TABLE 4-1. MINIMUM SELECTION CRITERIA (Continued)

Parameter Classification	Selection Parameter	Optimum Value From Survey	Minimum/Maximum Value for Significant Use	Comments
7. Decoding	a. I/O	TTL and/or CMOS compatible	TTL and/or CMOS compatible except for clock.	MACI requires column 25 minimum.
8. Availability	Commercial Parts Policy	High Rel to MIL STD 883-B	Commercial parts open to all Defense contractors.	MACI regquires parts be available to all at device level.

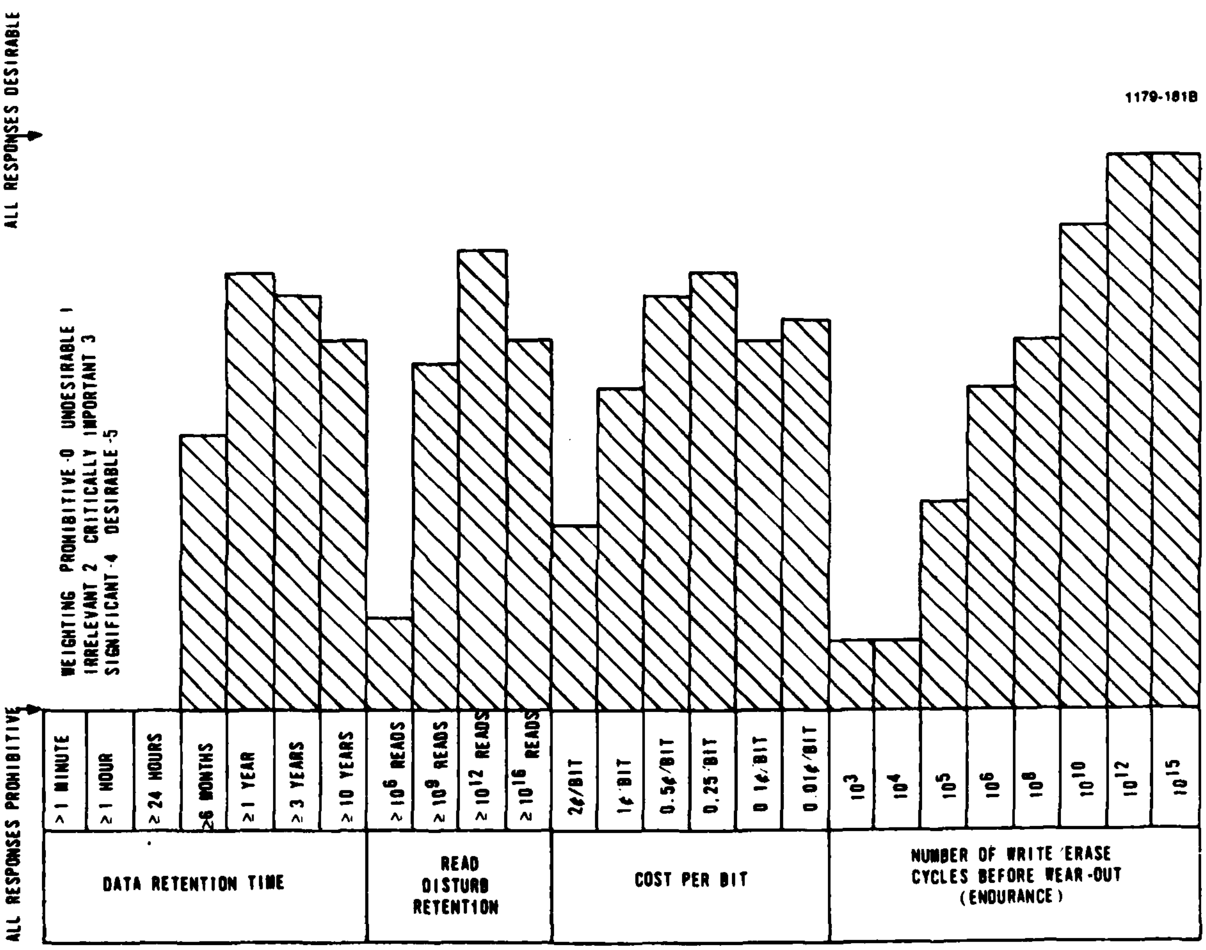


FIGURE 4-3. SIGNIFICANT PARAMETERS

Other aspects considered in the selection process were related to the vendor such as:

- Device availability both presently and potential in the future
- Production capacity with respect to demand
- Level of vendor support of device
- Yield and its influence on future support
- Multiple sources
- Quality control levels such as inspection procedures, in-process controls, and potential for high-reliability production
- Domestic sources
- Viability of manufacturer.

4.3 Vendor Data

All potential MNOS device manufacturers who met device availability requirements and had devices that were suitable for the MACI program were visited and surveyed. Vendors found willing and able to meet MACI requirements were:

- NCR - National Cash Register of Miamisburg, Ohio.
- GI - General Instruments of Hicksville, N.Y.
- Nitron Corporation of Cupertino, CA.

Devices found to be suitable for MACI program evaluation were:

- NCR - 2401, 2451, 2810
- GI - ER2401, ER3400, ER2810
- Nitron - NC7053, NC7054, NC2810.

Some of these parts were not available at the start of MACI (July 1978) and thus were added by relationship to similar parts made by other manufacturers (i.e., ER2810 and NC2810 were added after examination of NCR2810 parts).

Inspection procedures for all vendors were compared to MIL-STD-883-B methods as shown in excerpts of the MACI First Interim Report, Table 6-1 shown in Table 4-2 below. By displaying the vendor inspection procedures point for point against MIL-STD883-B, easy comparisons of procedure could be made.

In addition to quality procedures, vendor price and delivery data was presented. Figure 4-4 shows a graph of the delivery performance of each of the vendors for parts ordered for the MACI program. This section concluded with the most likely candidate devices being:

- NCR2810 - 8K EAROM, 2K words x 4 bits/word
- GI - ER2810 - Same as above
- GI - ER3400 - 4K WAROM - 1K words x 4 bits/word
- NCR - 2451 - Same as above.

Other devices tested but considered to have lower potential due to single source or waning support were:

- ER2401/NCR2401 - 4K EAROM - 1K words x 4 bits/word
- Nitron NC7053 - 1K WAROM - 256 words x 4 bits/word.

Schematic diagrams of several devices were shown for reference.

4.4 Performance Characteristics

Each of the candidate devices was then characterized for normal memory device function performance. Unique MNOS performance parameter characterizations were covered in a special section.

Using typical waveshapes as shown in Figure 4-5 and a special data pattern developed for EAROMs in the MACI program (Figure 4-6, Assymetric Slant), all devices were characterized for read access variation due to temperature and bias. Typical results are shown in Figure 4-7 which presents bias/read access schmoo diagrams for selected temperature ambients for the NCR2451 WAROM. Figure 4-8 shows a composite diagram of average access time versus temperature for all candidate devices.

Other performance parameters characterized were device power supply current dissipation versus temperature and current wave shapes for each device. In this section, a preliminary look at the radiation resistance characteristics was taken. Figures 4-9 and 4-10 show the normal threshold plot against time of a GI ER3400 with the affects of an X-ray shot superimposed after 10^5 seconds from write.

TABLE 4-2. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
b. Unattached foreign material on the surface of the lid or cap. NOTE: Criteria of 3.2.6.1 can be satisfied by a nominal gas blow (approximately 20 psig) or a suitable cleaning process providing that the lids or caps are subsequently held in a controlled environment until capping.		
c. Attached conductive foreign material that bridges metallization paths, package leads, lead to package metallization, functional circuit elements or junctions, or any combination thereof. NOTE: Glassivated areas of the die can be excluded from the criteria of 3.2.6.1 c when the particle or material is attached only at the top surface of the glassivation.	b. Attached conductive foreign material on the top of the die and under the silox that bridges two or more metal lines. (NOTE: Attached foreign material on top of silox is not rejectable.	Vendor's criteria does not include functional circuit elements or junctions.
d. Ink on the surface of the die that covers more than 25 percent of a bonding pad area or that bridges any combination of unglassivated metallization or bare silicon area.	e. Opaque attached particles large enough to bridge any two package leads, or any lead to package metallization or a bonding pad to the edge of the die.	
	c. A clear liquid appearance on top of the silox.	
	d. Fingerprints or oily droplets	Vendor's criteria does not include all of the respective 883 criteria.
3.2.6.2 <u>Die Mounting</u>	3.2.7 <u>Die Mounting (30X to 50X)</u>. No device will be acceptable which exhibits:	
a. Die mounting material buildup that extends onto the top surface of the die.	a. Die mounting material buildup that touches the top surface of the die.	
b. Die to header mounting material not visible around at least 50 percent of the die perimeter or continuous on two full sides of the die, whichever is less, except for transparent die.	b. Die to header melt not visible around 75 percent of the die perimeter and continuous on two sides.	Vendor's criteria exceeds 883B
c. Transparent die with less than 50 percent of the area bonded.		
d. Flaking of the die mounting material.		
e. Balling of the die mounting material that does not exhibit a fillet, when viewed from above (see Figure 2010-30).	c. Balling or flaking of the die mounting material.	
3.2.6.3 <u>Die Assembly</u>. Die not located and oriented in accordance with the applicable assembly drawing of the device.	d. Die not located or oriented in accordance with the applicable assembly drawing of the device.	
3.2.7 <u>Glassivation Defects, "High Magnification"</u>. No device shall be acceptable that exhibits:		
a. Crazing that prohibits the detection of visual criteria contained herein.		

TABLE 4-2. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
b. Any lifting or peeling of the glassivation. NOTE: Lifting or peeling of the glassivation may be excluded from the criteria above, when it does not extend more than 0.001 inch distance from the designed periphery of the glassivation, provided that the only exposure of metal is of adjacent bond pads or of metallization leading from those pads.		
c. Two or more adjacent active metallization paths not covered by glassivation, excluding bonding pad cutouts.		
d. Unglassivated areas greater than 5.0 mils in any dimension, unless by design.		
e. Unglassivated areas at the edge of bonding pad exposing silicon.		
f. Glassivation covering more than 50 percent of the bonding pad area.		
g. Crazing over a film resistor.		
3.2.8 <u>Dielectric Isolation "High Magnification"</u>. No device shall be acceptable that exhibits:		
a. A discontinous isolation line (typically a black line) around each diffusion tub containing functional circuit elements (see Figure 2010-31).		
b. Absence of a continuous isolation line between any adjacent tubs containing functional circuit elements.		
c. A diffused area which overlaps dielectric isolation material and comes closer than 0.1 mil to an adjacent diffusion tub; or an overlap of more than one diffusion area into the dielectric isolation material (see Figure 2010-31).		
d. A contact window that touches or overlaps dielectric isolation material.		
e. Metallization scratch and void defects over a dielectric isolation step shall be in accordance with criteria in 3.2.1.1 b and 3.2.1.2 b.		
	3.2.8 <u>Package Post Metallization Defects (30X to 50X)</u>. No device shall be acceptable which appears to exhibit the following:	
	a. Post to post bridging which reduces the metallization separation to less than 25 percent.	
	b. Post voids which reduce the metallization width to less than 50 percent in the first 15 mils nearest the die.	

TABLE 4-2. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences

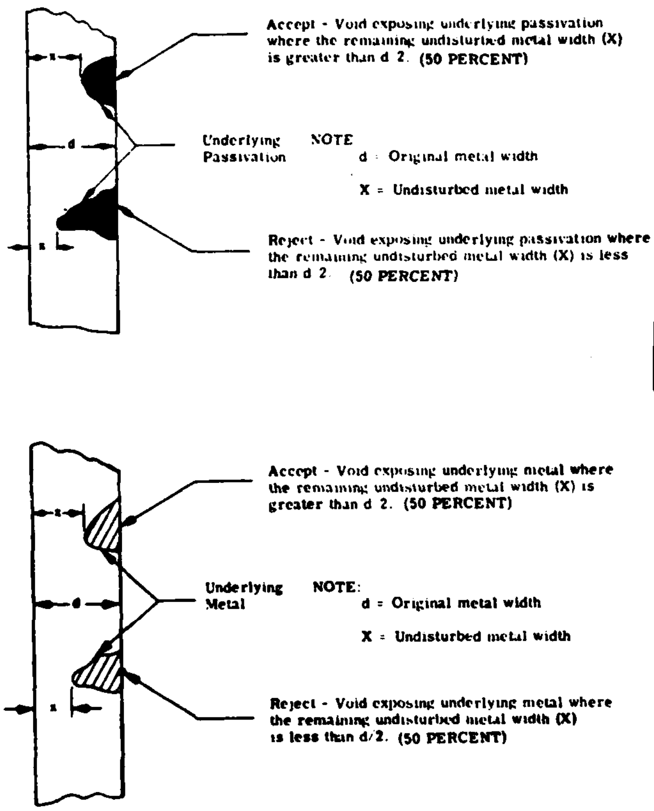


FIGURE 2010-19. VOID CRITERIA

VOID CRITERIA

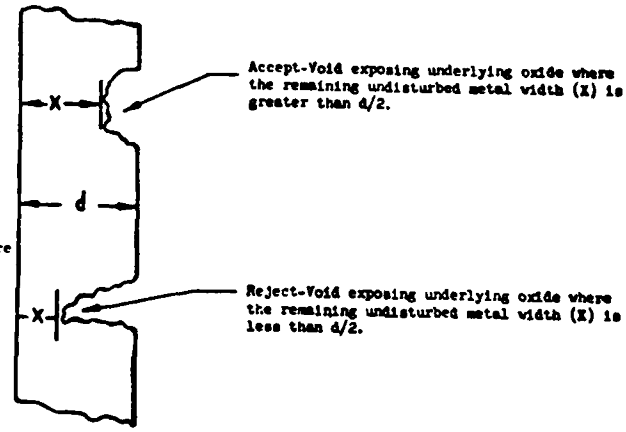


FIGURE 3

TABLE 4-2. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences

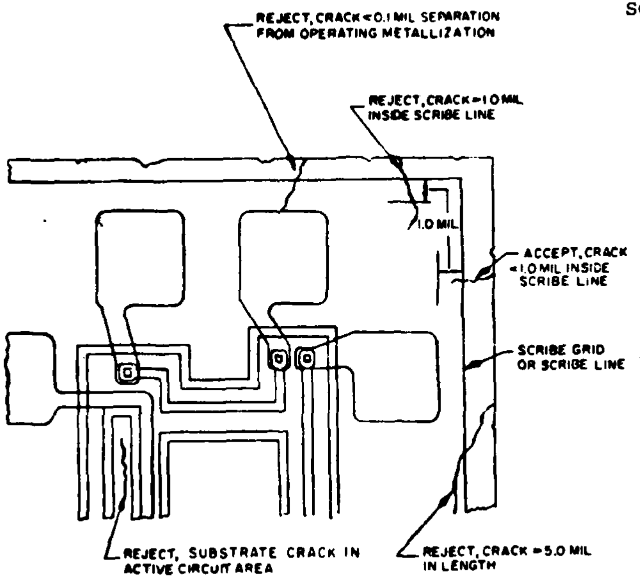


FIGURE 2010-24. SCRIBING AND DIE DEFECTS

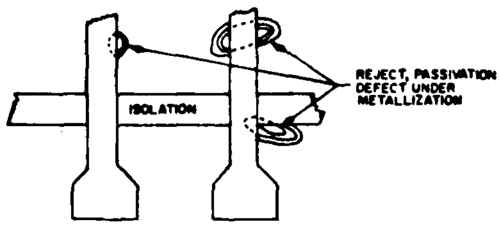


FIGURE 2010-23. PASSIVATION FAULT

SCRIBING AND DIE DEFECTS

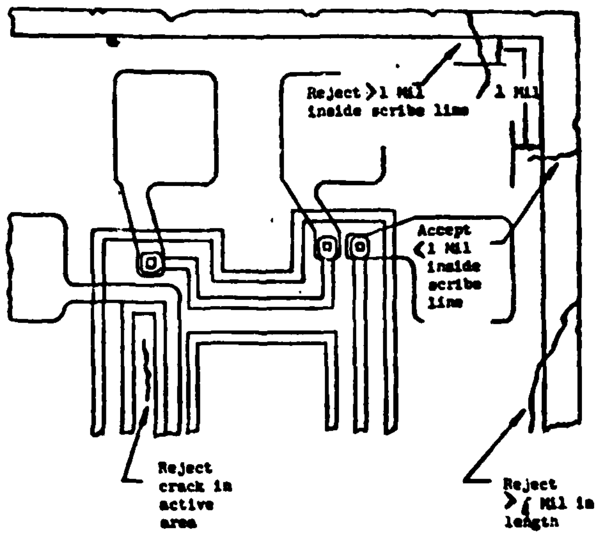
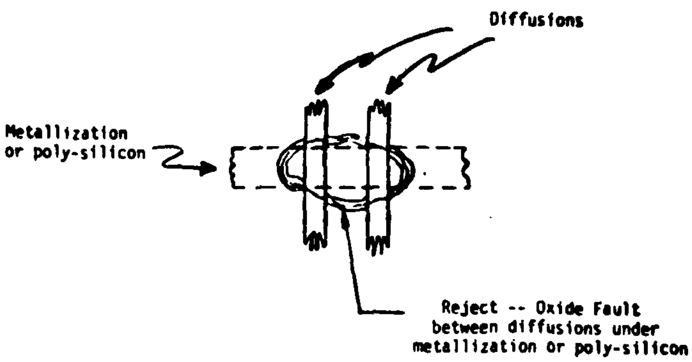


FIGURE 1

OXIDE FAULTS



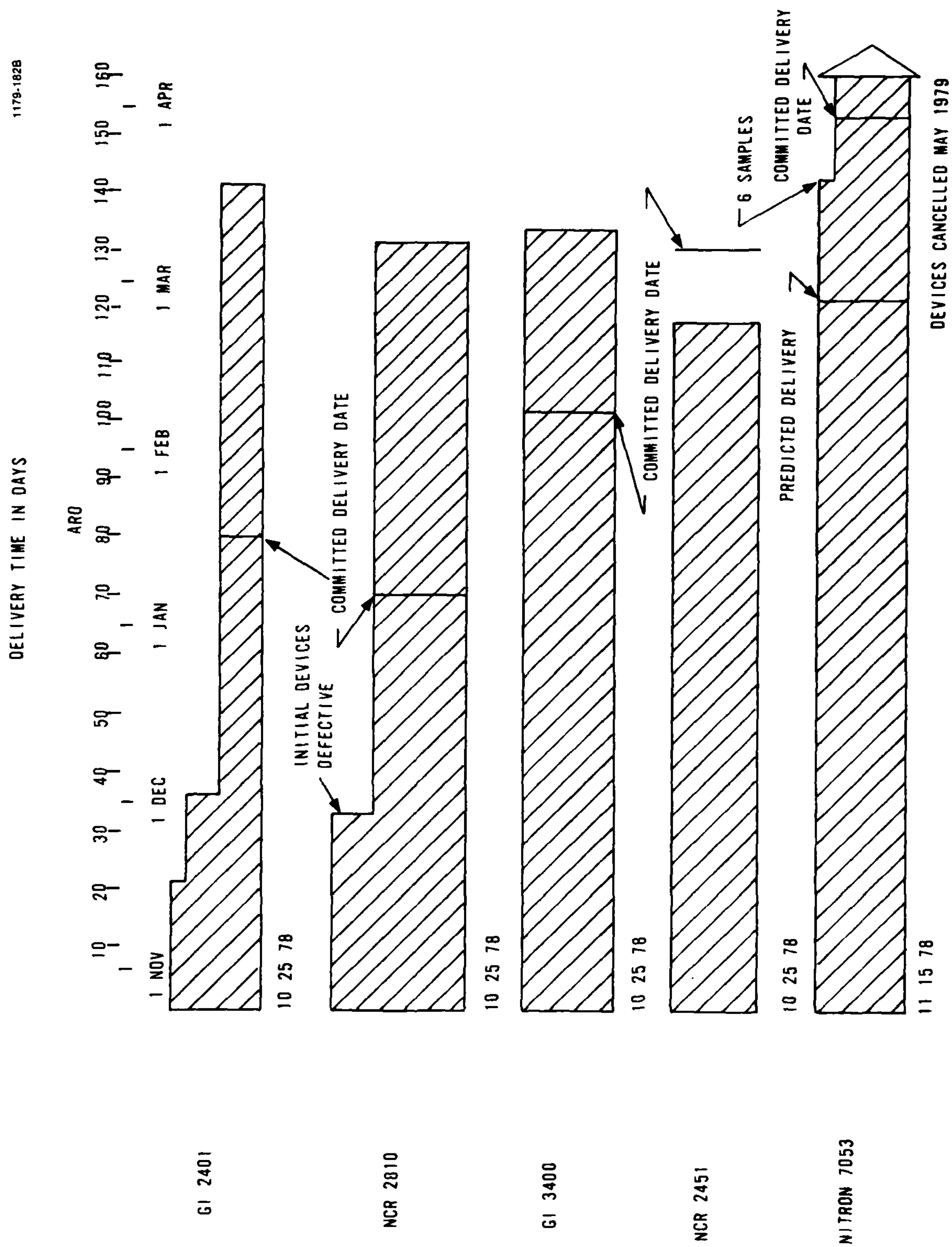
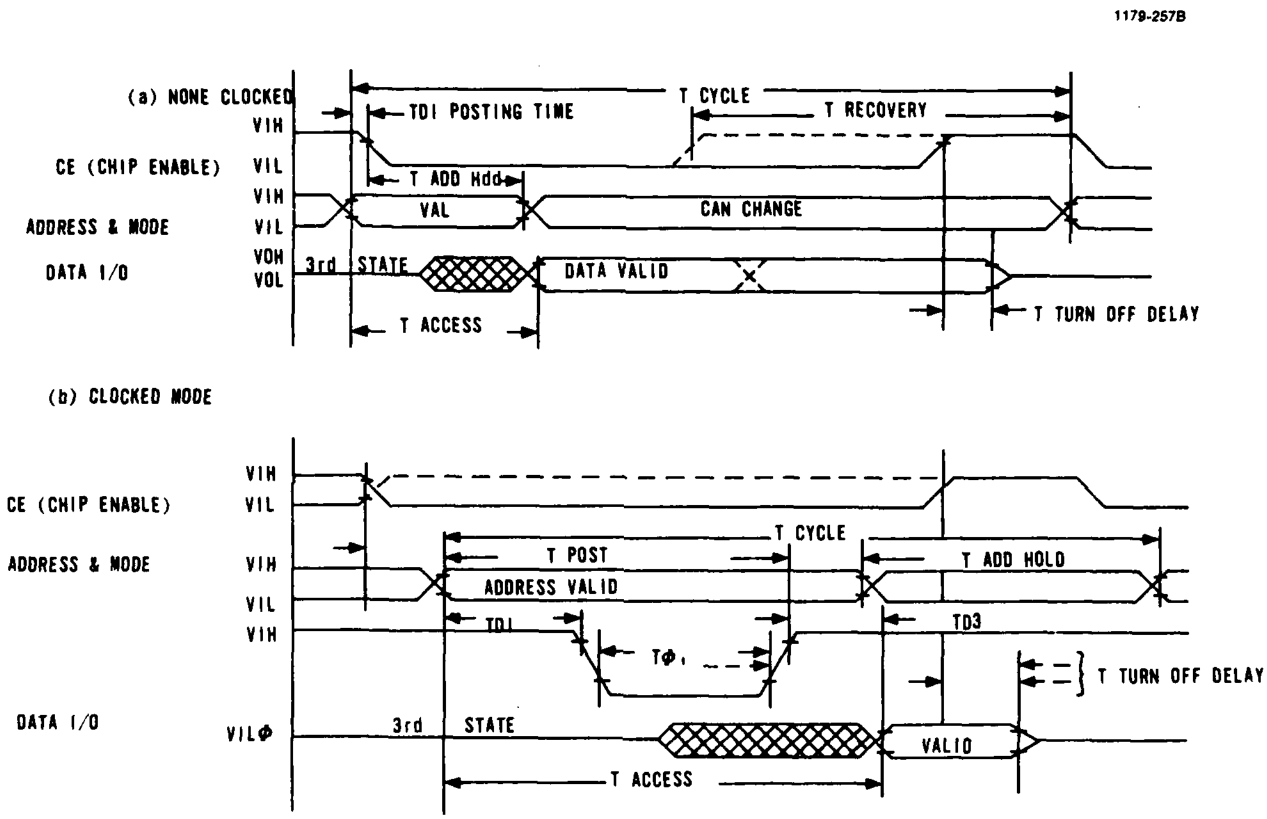


FIGURE 4-4. - DELIVERY TIME IN DAYS



NOTE: THIS DIAGRAM DOES NOT REPRESENT ALL MNOS DEVICE READ WAVESHAPES BUT IS TYPICAL OF THEIR OPERATION. SEE VENDOR SPEC FOR DETAILS OF SPECIFIC DEVICE

FIGURE 4-5. TYPICAL READ CYCLE WAVE SHAPES

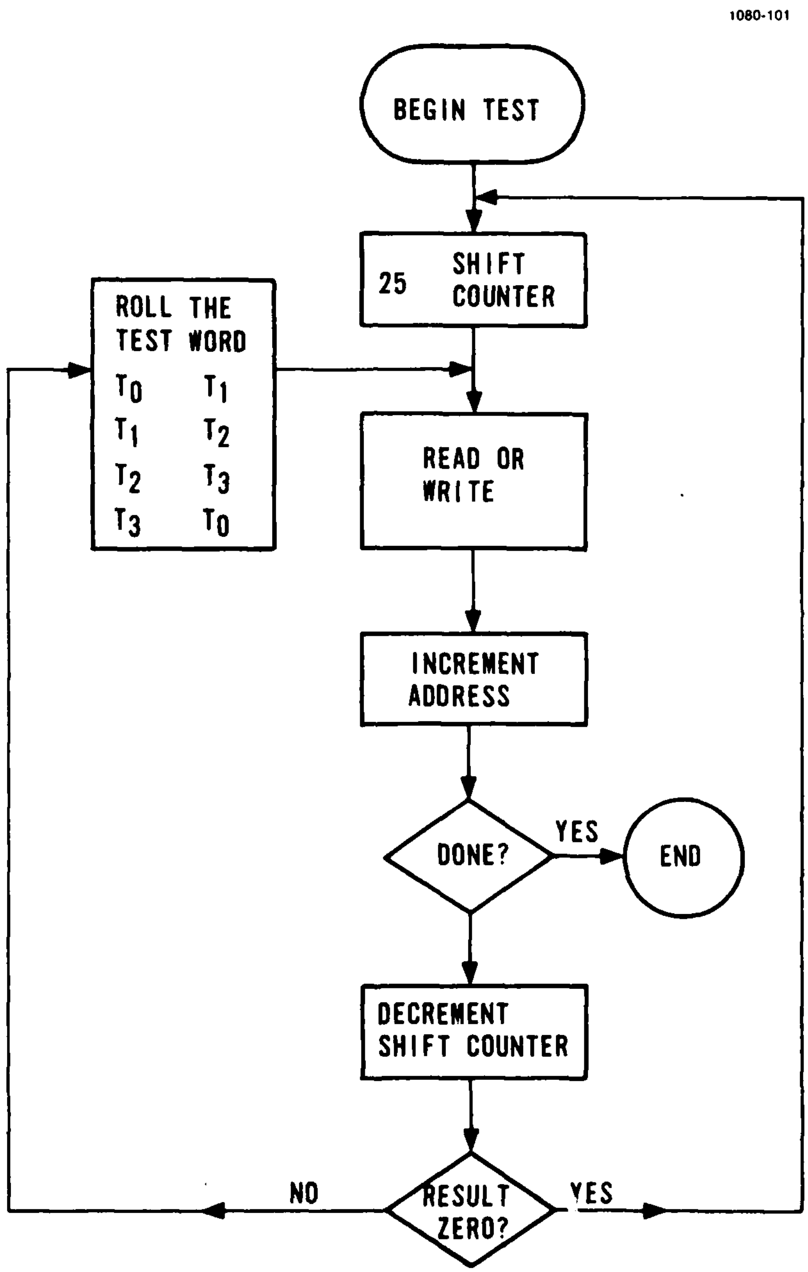


FIGURE 4-6. ASYMMETRIC SLANT ALGORITHM

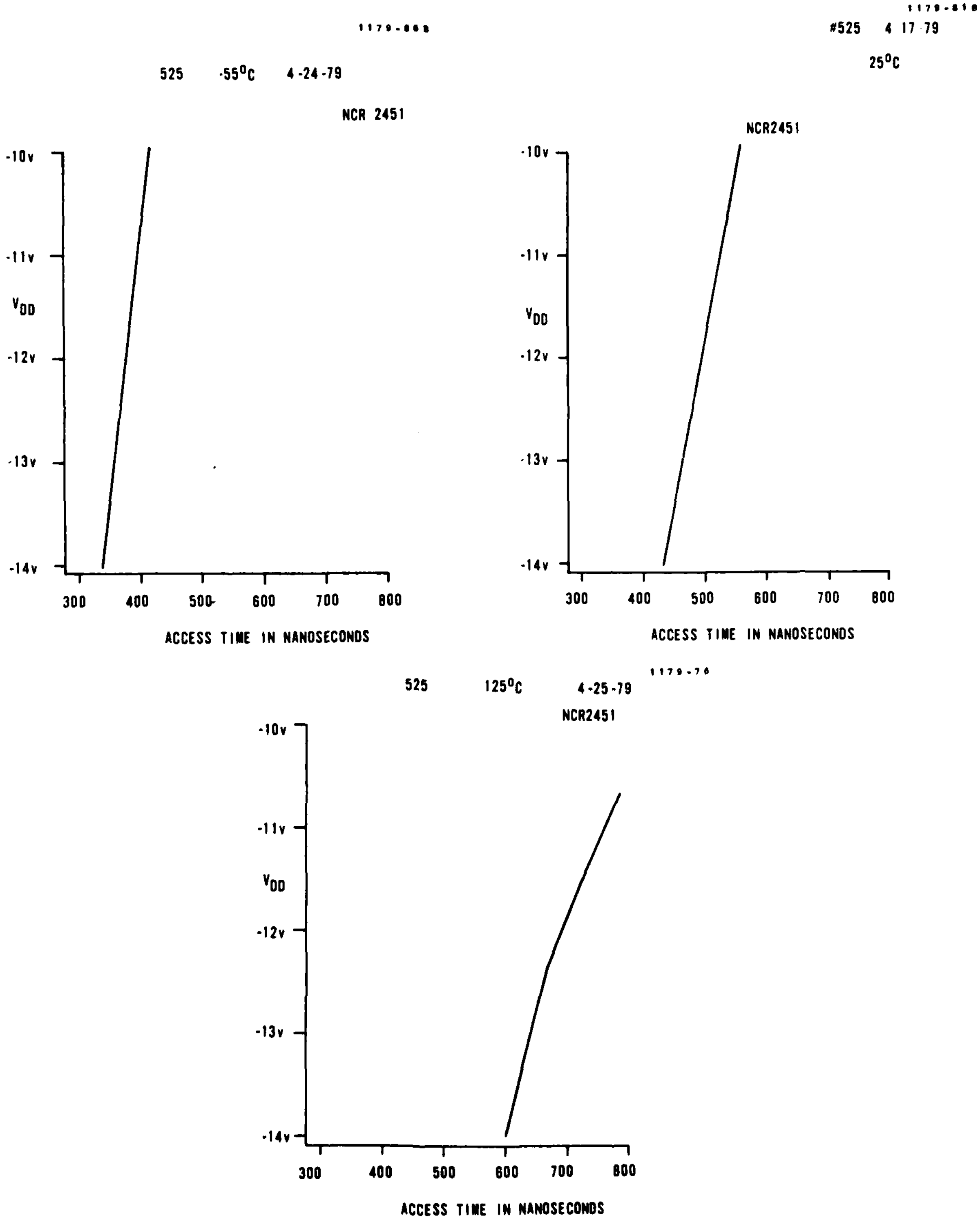


FIGURE 4-7. ACCESS TIME CHARACTERISTIC OF NCR 2451

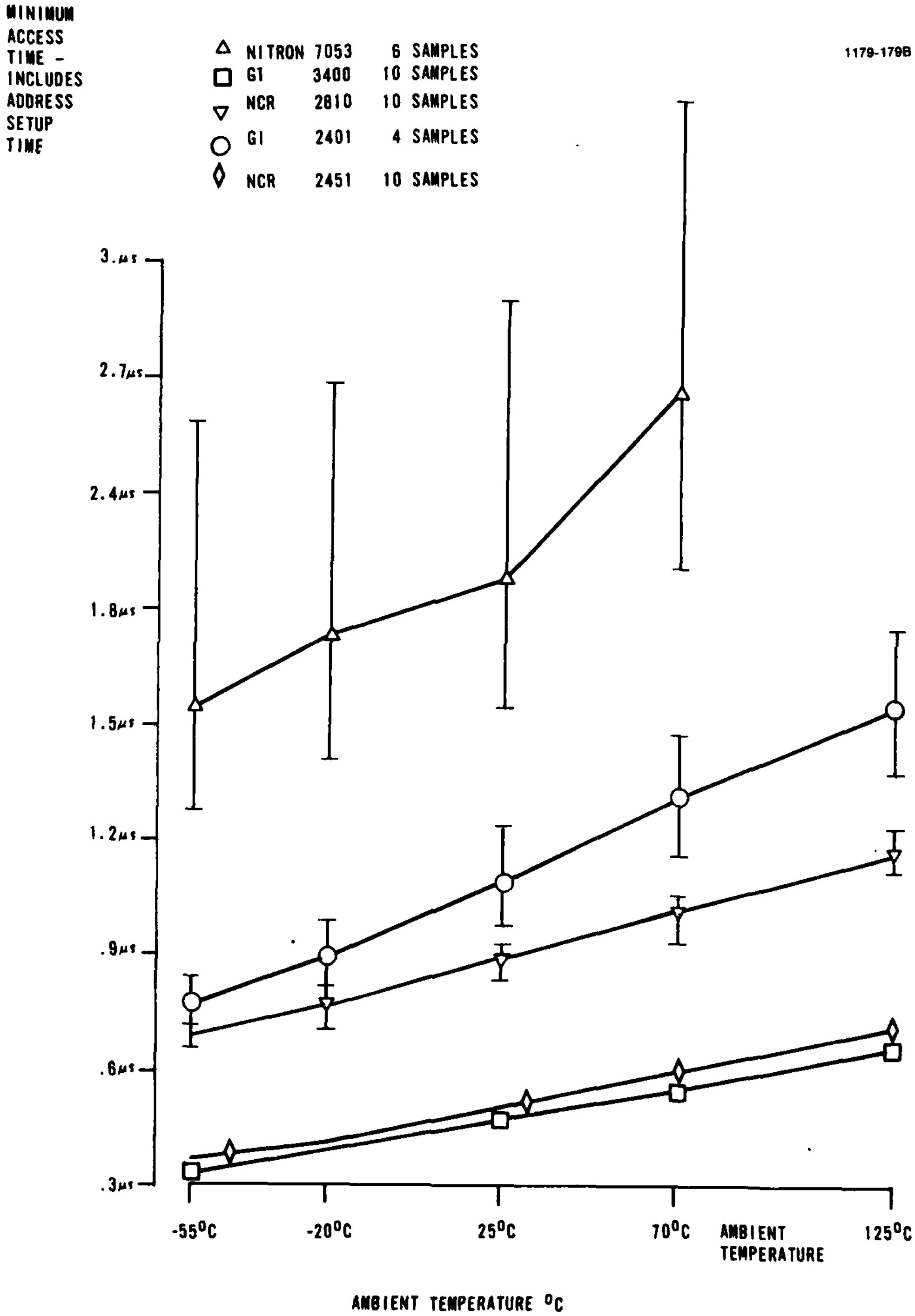


FIGURE 4-8. ACCESS TIMES COMPOSITE

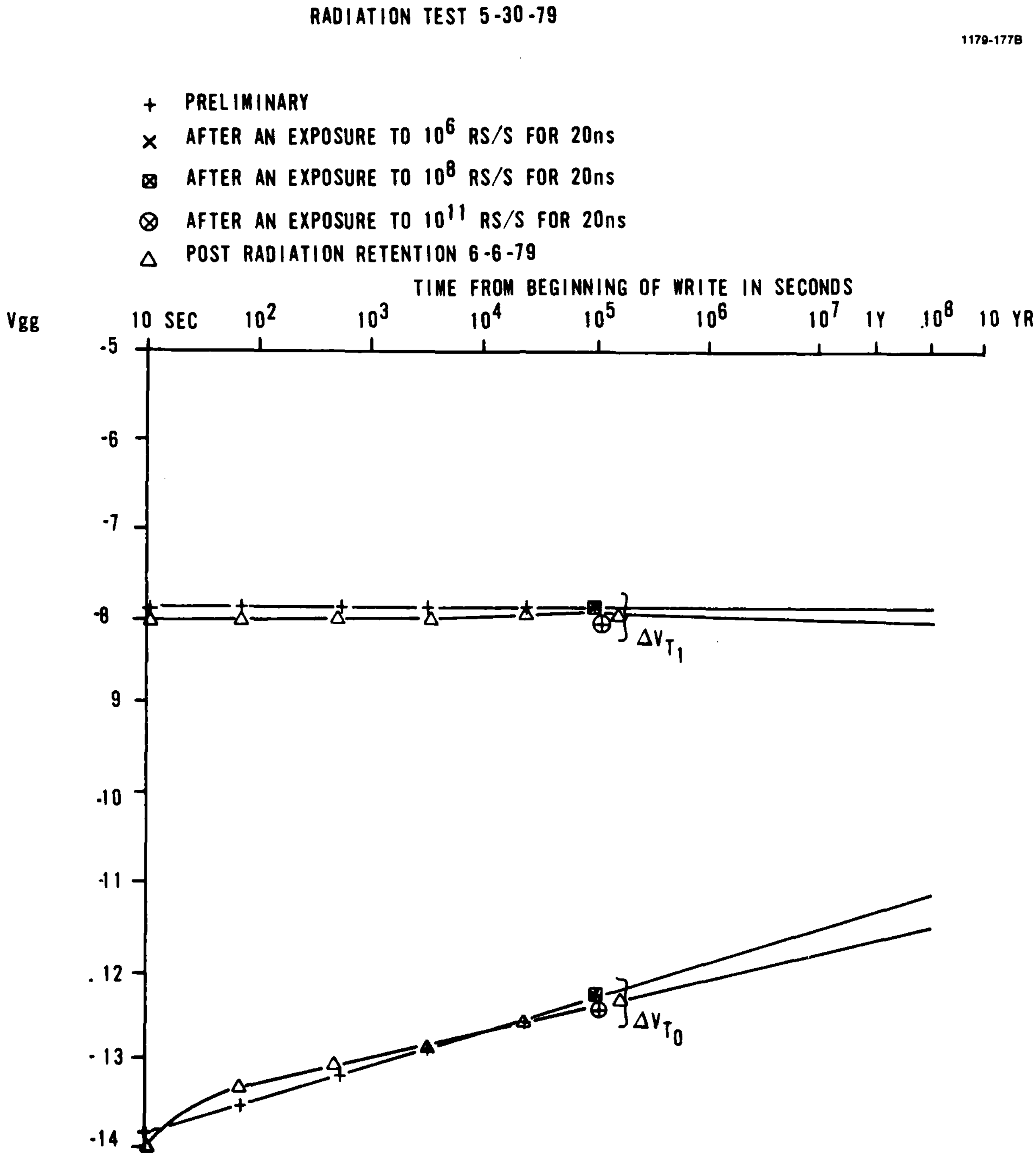


FIGURE 4-9. RADIATION EXPOSURE TESTING OF GI3400 (SHORT CIRCUIT UNBIASED STATE)

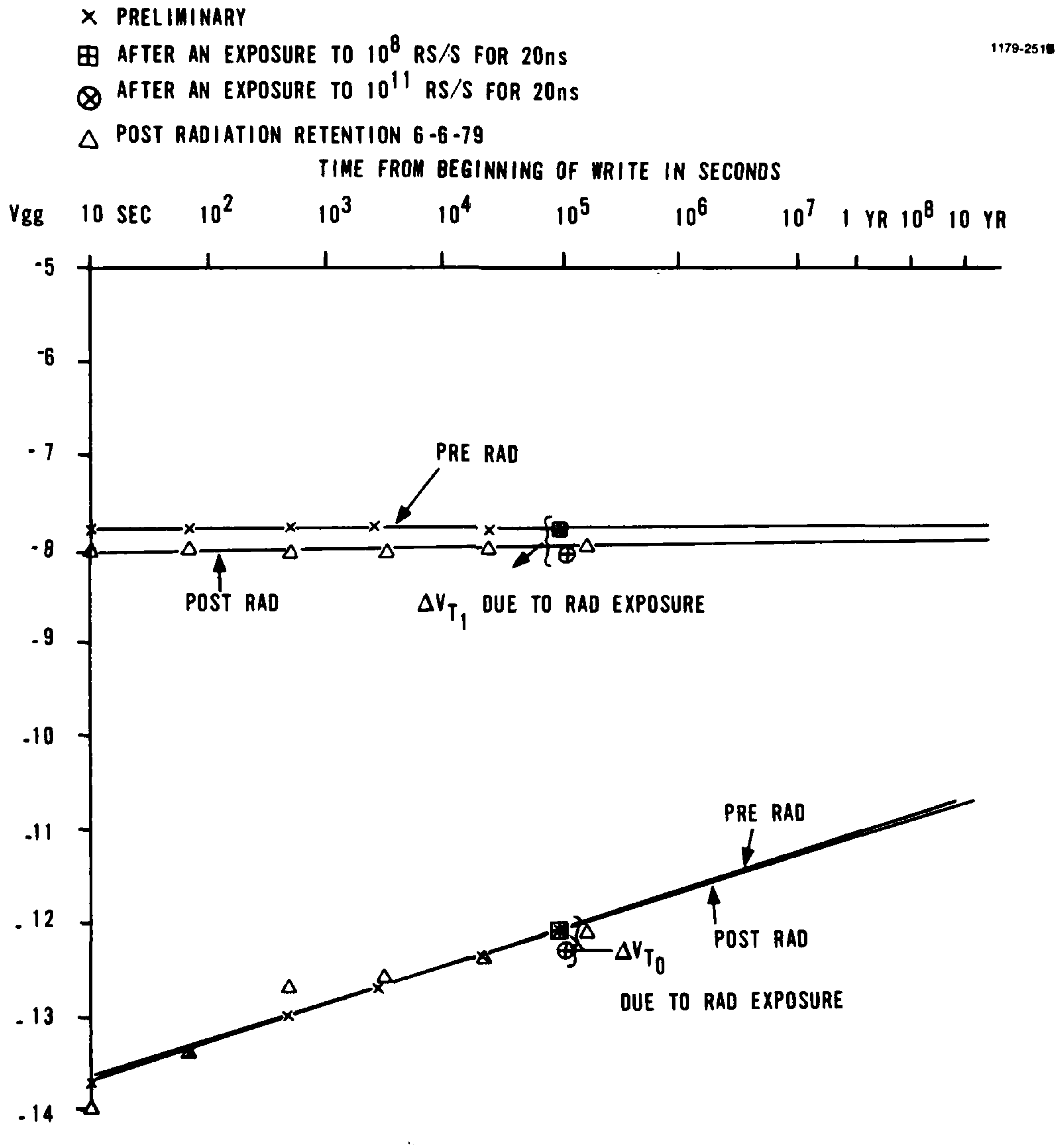


FIGURE 4-10 . RADIATION EXPOSURE TESTING OF GI3400 (BIASED STATE)

Figure 4-9 shows this plot with the device unbiased when exposed to X-ray and Figure 4-10 shows it in the biased state. As can be seen, there was little affect on the device thresholds or device operation for X-ray dose rates of up to 10^{11} rad si/sec (20 ns). Table 4-3 shows the results on all devices tested with X-ray exposure in this phase of the program.

4.5 Unique MNOS Characteristics

These characteristics of Retention, Read Disturb Retention, and Endurance, as defined on Page 8-1 of the First Interim Report, are parameters that require special attention when evaluating MNOS devices. Since there are no current formal definitions or completely accurate circuit models, those definitions given are to some degree ambiguous and subject to official refinement. However, for the purposes of defining and measuring these parameters for the MACI program, these definitions were used.

The ability to measure memory device thresholds is very significant in developing methods of performing accelerated or predictive retention tests. While methods have been developed to perform accelerated retention tests for devices where threshold measurement is not available, the correlation of these methods to actual real time retention is questionable.

Using threshold plotting, it is seen in Figure 4-11 that the rate of discharge of the memory cell is logarithmic with time which is a direct relationship with the transistor threshold voltage. By plotting voltage threshold against time on a lin-log graph, the end of retention point can be predicted by extrapolating on a graph by means of a best fit line until it crosses the reference voltage line or approaches the opposite sense line within the sense amp sensitivity. Figure 4-11 shows plots of a typical MNOS device under four different conditions. Table 4-4 illustrates the results of typical devices of four of candidate device types with the retention predictions based on best fit lines. The correlation coefficient of these lines to the actual measurements is shown. Detailed explanation of the actual method of prediction was shown in the Third Interim Report.

The second of these parameters, Read Disturb Retention, is loosely tied to the first. This parameter addresses itself to the effect of potentially changing the state of data within the memory by reading individual locations a greater number of times than the specification allows. The effect works like a very soft write which with the devices tested tends to disturb the "1"s (low threshold) and enforce the "0"'s (hi threshold). Figures 4-12, 4-13 and 4-14 show the effects of read disturb. Figure 4-12 illustrates the read

TABLE 4-3. RESULTS OF RADIATION TESTING OF MNOS DEVICES FOR MACI - EAROM PROGRAM

Device	Rad Exp.	Total Dose	Initial V_T Ones	Initial V_T Zeros	Change V_T Ones	Change V_T Zeros	Retention Pre	Retention Post	Average Change V_T/Decade-Zeros Pre	Average Change V_T/Decade-Zeros Post
2401 #406	10^6/sec	0.02	0.58	-5.14	0	0				
	10^8/sec	2.02	0.58	-5.14	-0.2	0	1.49 x10^{20}	1.72 x10^{20}	0.2774	0.2763
	10^{11}/sec	2002.02	0.56	-5.14	0	0.033				
2501 #507	10^6/sec	0.02	-7.7	-12.48	0	0.02				
	10^8/sec	2.02	-7.7	-12.45	0.02	0.01	1.15 x10^{11}	2.36 x10^{11}	0.4584	0.4773
	10^{11}/sec	2002.02	-7.88	-12.72	-0.22	-0.28				
3400 #217	10^8/sec	2.0	-7.8	-12.1	0	0.02	4.75 x10^9	5.01 x10^9	0.4237	0.3700
	10^{11}/sec	2002.0	-7.8	-12.08	-0.22	-0.18				
2810 #334	10^6/sec	0.2	-4.14	-9.5	0	0				
	10^8/sec	2.02	-4.14	-9.5	0	0.02	4.19 x10^{14}	8.28 x10^{14}	0.4143	0.4207
	10^{11}/sec	2002.02	-4.14	-9.48	-0.02	0.08				

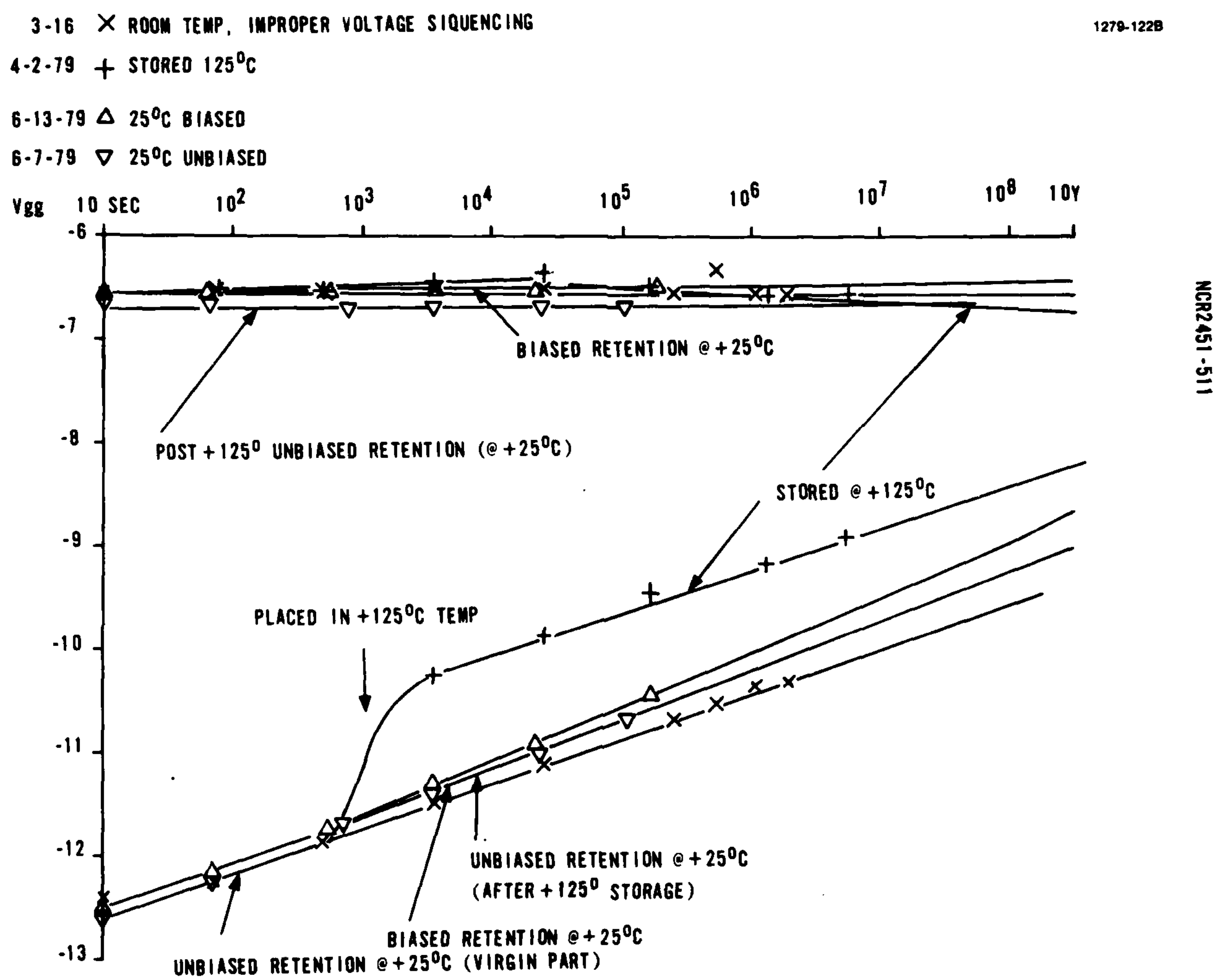


FIGURE 4-11. TYPICAL RETENTION PREDICTION PLOTS OF NCR2451

TABLE 4-4. RETENTION RESULTS

Device Serial	Initial Retention Cr Co*	Initial Retention Decay Rate	125°C Retention Cr Co*	125°C Retention Decay Rate	Off-Set at 10^3	After 125°C Retention Cr Co*	After 125°C Retention Decay Rate	Biased Retention Cr Co*	Biased Retention Decay Rate	Comments
2810										For 125°C test, devices written at temperature.
318	2.06×10^{12} -0.9979	-0.473	4.40×10^{9} -0.9988	-0.543	N/A	No Test		2.03×10^{12} -0.9975	-0.493	
319	1.98×10^{14} -0.9977	-0.382	1.07×10^{11} -0.9994	-0.442	N/A	No Test		7.36×10^{14} -0.9997	-0.376	
2401 412	4.74×10^{18} -0.9961	-0.299	1.02×10^{17} -0.9974	-0.293	0.843	1.48×10^{23} -0.9874	-0.255	9.55×10^{21} -0.9950	-0.269	Better retention after 125°C reflects a refinement of test procedure to minimize glitchs occurring at the initial-ization of MD-150 statewords.
415	1.25×10^{18} -0.9771	-0.266	4.48×10^{12} -0.9946	-0.360	0.599	1.78×10^{19} -0.9993	-0.262	2.03×10^{20} -0.924	-0.248	
2451 511	1.73×10^{10} -0.9976	-0.426	1.66×10^{7} -0.9999	-0.447	1.278	3.75×10^{9} -0.9996	-0.463	8.28×10^{8} -0.9987	-0.503	Poorer retention after 125°C leads one to suspect a temperature related degradation of retention characteristic.
513	3.95×10^{10} -0.9999	-0.445	1.76×10^{8} -0.9957	-0.376	1.413	8.41×10^{9} -0.9994	-0.462	1.66×10^{9} -0.9991	-0.505	
3400 207	1.15×10^{11} -0.9976	-0.309	3.08×10^{8} -0.9940	-0.297	1.232	No Test		No Test		Reference Voltage: -9.44 Decay at 125°C
2.09	1.17×10^{10} -0.9966	-0.353	1.16×10^{8} -0.9901	-0.305	1.298	No Test		No Test		Reference Voltage: -9.90

*Cr Co - Correlation Coefficient

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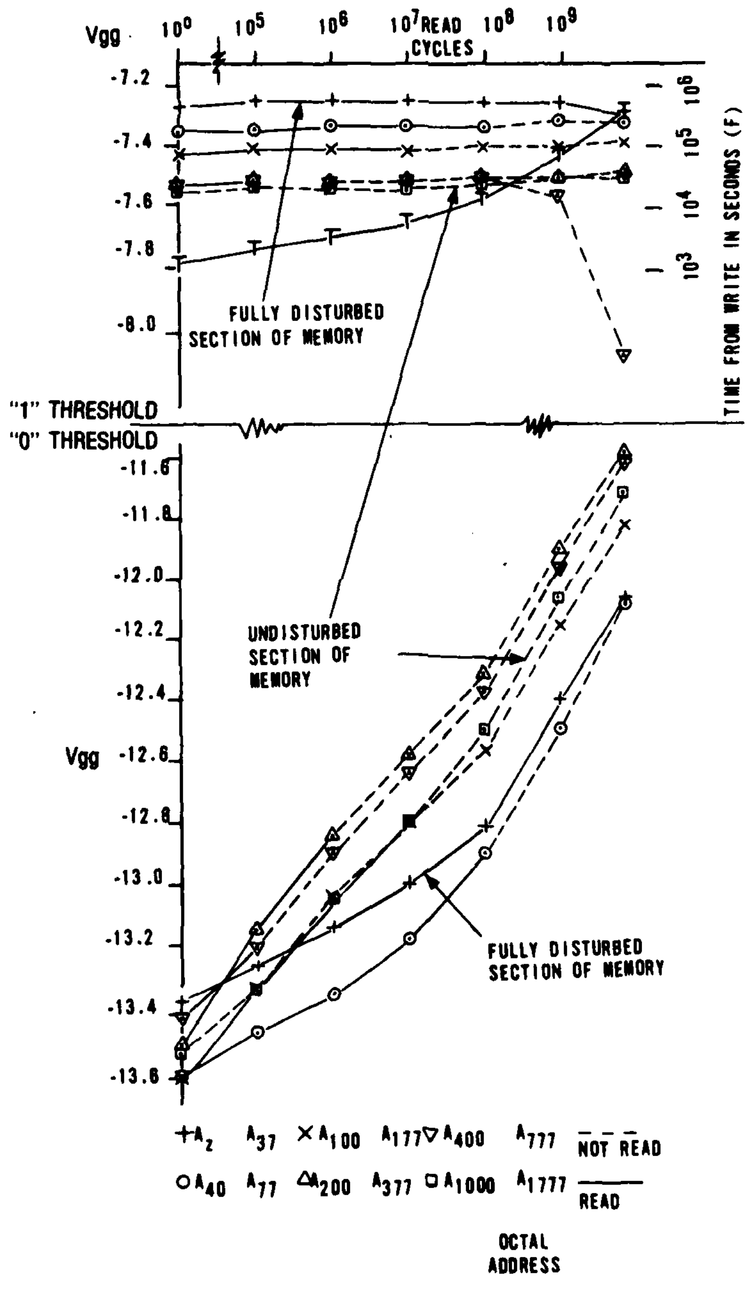

FIGURE 4-12. READ DISTURB RETENTION OF NCR 2451
(Immediately after Write)

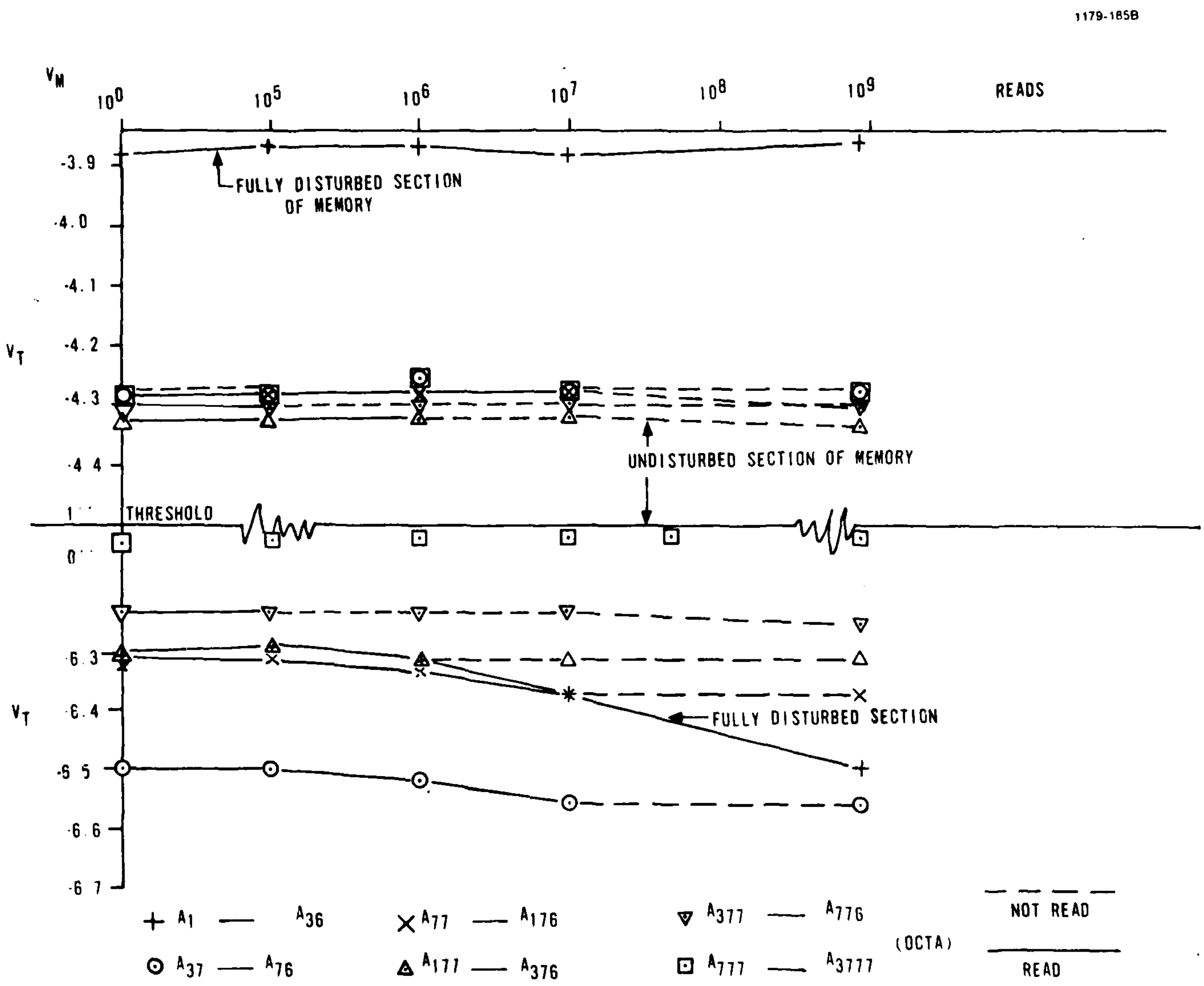

FIGURE 4-13. READ DISTURB RETENTION ON NCR 2810
AFTER 24 DAYS OF STORAGE @ +25°C

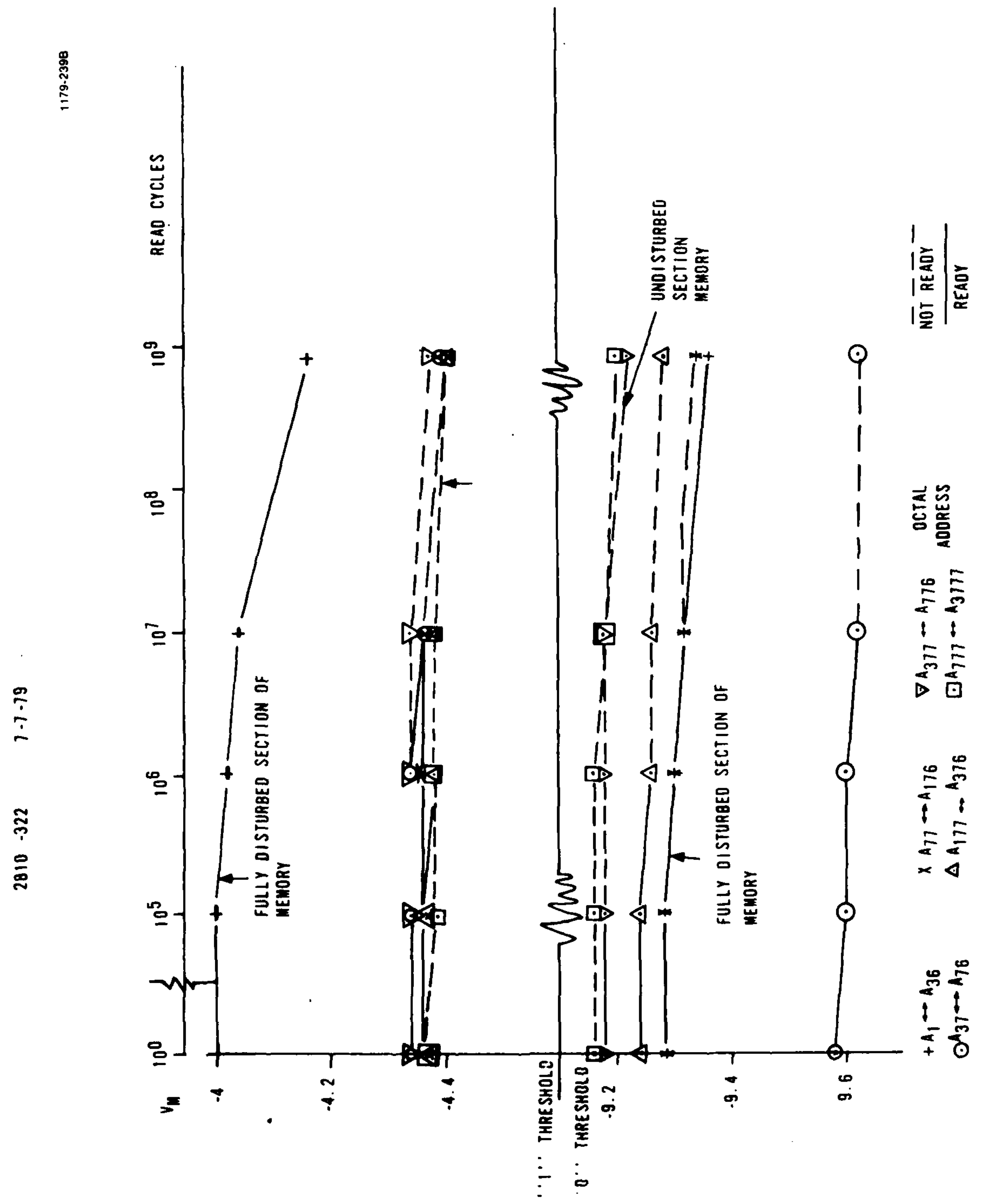

FIGURE 4-14. READ DISTURB RETENTION ON NCR 2810
AFTER 109 DAYS OF STORAGE AT +25°C

disturb effects on a device being constantly read immediately after writing. The "0" thresholds, while changing rapidly at this point show decreasing decay rates for sections being read (i.e., enhanced "0" effect). The "1" threshold is not affected by the read disturb here due to the threshold being controlled by thick oxide regions of the transistor masking the thin oxide Vt change effect. In Figure 4-13, the enhancement of the "0" threshold is clearly seen by the negative slope of the disturbed sections of memory. The "1" threshold is still not being affected by read disturb for the same reasons as above. In Figure 4-13, however, the "1" threshold can be seen to decay at a more rapid rate for the disturbed portion of memory while the "0" Vt is still being enhanced.

The "1" Vt in this case has discharged to a level where the thin oxide region is controlling the device threshold and being "written down" by the read disturb effects.

The third unique MNOS parameter to be examined was the Endurance characteristic. This parameter addresses the change in static retention as a function of the number of erase/write cycles performed on a particular location. While measuring of this characteristic is normally a destructive test, some methods of performing predictive nondestructive tests were developed for the MACI program.

Figure 4-15 shows the changing nature of the retention as a function of the number of erase/write cycles performed. Out of the initial lot of NCR 2810 devices, this device exhibited better endurance than most. It was predicted to show better endurance by performing a hard-write soft-erase cycle and measuring the minimum "0" threshold. This relates to speed of the erase function being inversely proportional to the nitride thickness. It has been noted that thicker nitride devices in any lot show better endurance than similar devices in the same lot with thinner nitride layers. Figure 4-16 shows an endurance plot (i.e., varied retention plots) of a "thinner nitride" part as measured by the erase characteristic. It shows the faster decay of the retention characteristic with erase/write cycling that was predicted. Table 4-5 shows the endurance characteristic of the NCR2810 devices and their relationship to the "soft Vt" measurement. Figure 4-17 plots these endurance measurements and shows the correlation to the "soft erase Vt" measurements. Figure 4-18 shows histograms of the "soft erase Vt" measurements, with the retention after $7x10^4$ E/W cycles superimposed. The correlation is clear; the upper histograms show a new lot of 2810 devices with thicker nitrides. The distribution on this lot indicates a significant improvement in endurance.

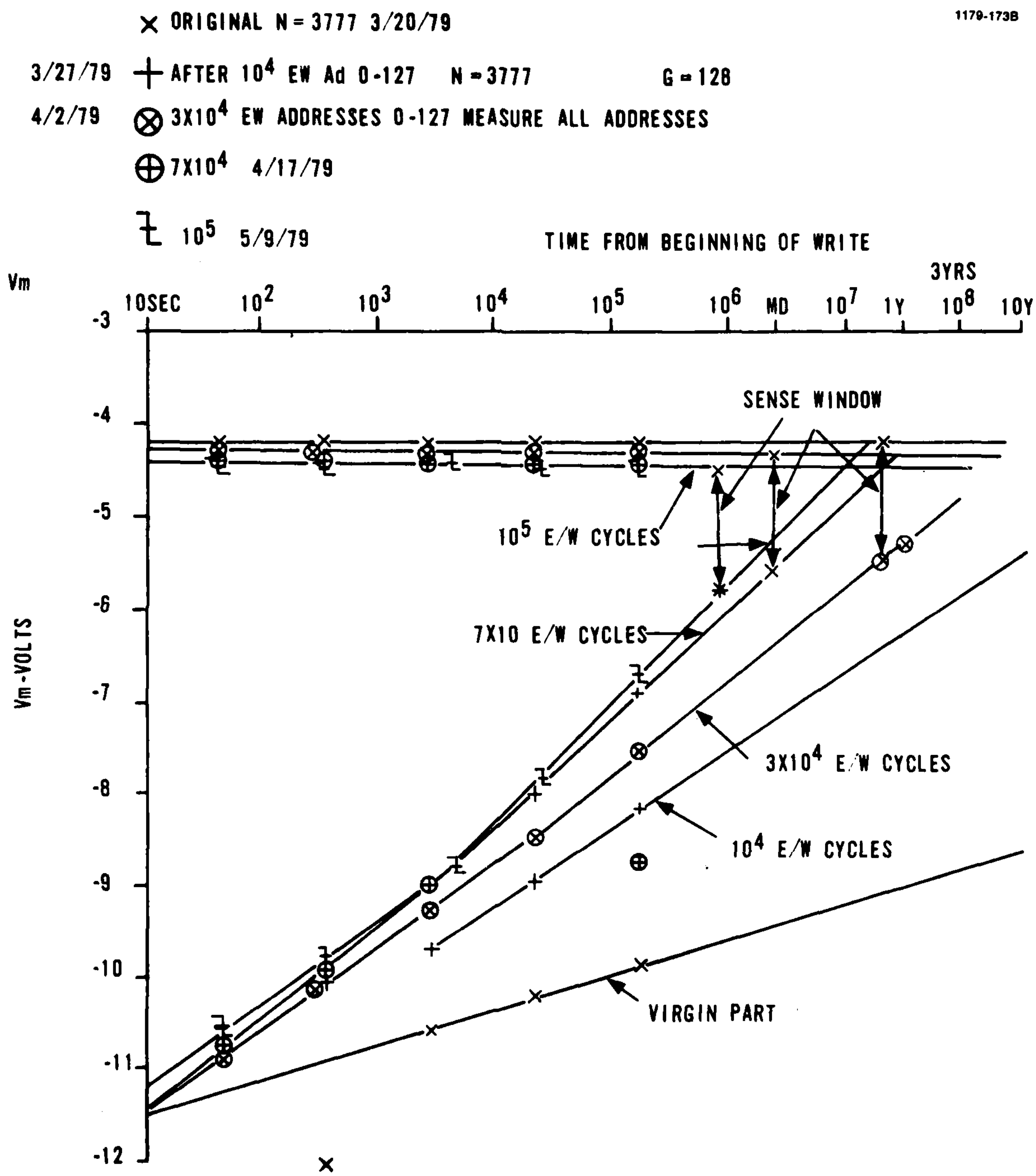

FIGURE 4-15. ENDURANCE OF NCR 2810
(RETENTION VS WRITE/ERASE CYCLES)

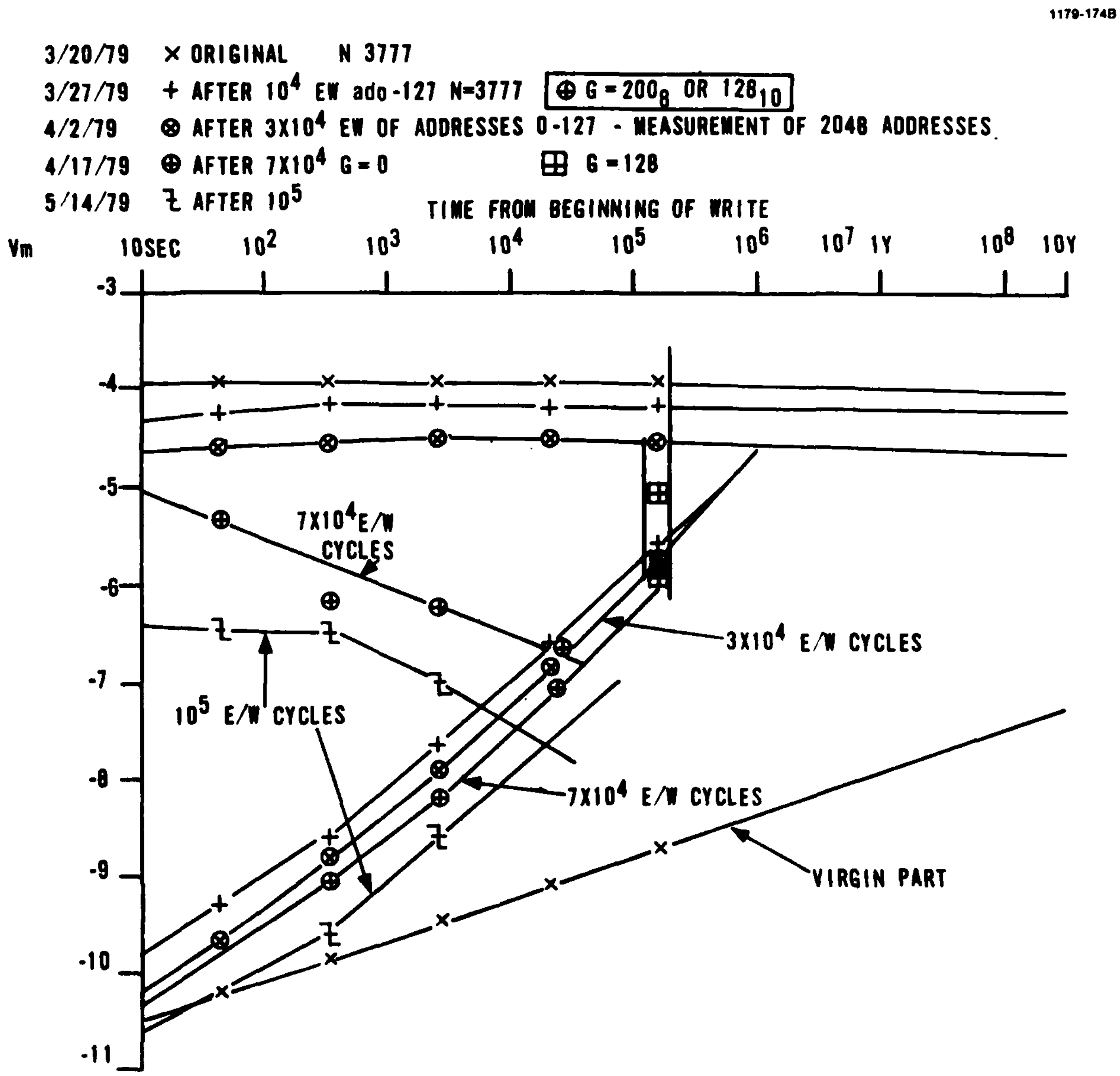

FIGURE 4-16. ENDURANCE OF NCR 2810
(INITIAL LOT - RELATIVELY THIN PART)

TABLE 4-5. ENDURANCE DATA FOR NCR 2810

Device	Reference Voltage	E/W Cycles	0 Bound Erased at -17V	16V Erases to Fail	Threshold Window at 44 seconds	Slope For Written State Threshold in Volts/Decade			Slope For Erased State Threshold in Volts/Decade			Normalized Retention at 1.4 Volts Window	Correlation Coefficient -1=linear
						Ave	Max	Min	Ave	Max	Min		
320 X		10^0	-12.73	125	6.38	0.445	0.467	0.423	0	0	0	4.02×10^{14}	-0.9996
		10^4			6.34	0.668	0.823	0.356	0.006	0.022	0	1.20×10^9	-0.9924
		3×10^4			6.66	0.983	1.05	0.895	0.017	0.025	0	1.43×10^7	-0.9997
		7×10^4			6.38	1.06	1.18	0.957	-0.021	0.022	-0.107	2.11×10^6	-0.9982
		10^5			6.12	1.08	1.27	0.824	0.012	0.026	0	1.76×10^6	-0.9954
323 O		10^0	-10.81	22	6.84	0.406	0.467	0.356	-0.006	0	-0.022	1.18×10^{15}	-0.9984
		10^4			6.12	0.952	1.16	0.623	0.006	0.022	0	5.22×10^6	-0.9925
		3×10^4			5.9	1.08	1.29	0.735	0.011	0.022	0	9.19×10^5	-0.9938
		7×10^4			5.78	1.14	1.32	0.757	-0.043	0.044	-0.216	2.70×10^5	-0.9931
		10^5			5.74	1.15	1.35	0.868	0.006	0.025	-0.045	3.86×10^5	-0.9966
327 ▽		10^0	-9.72	1	5.24	0.390	0.490	0.312	-0.006	0.022	-0.022	3.48×10^{11}	-0.9962
		10^4			---	1.20	1.36	1.05	-0.415	0	-0.829	6.44×10^3	-0.9799
		3×10^4			1.52	0.378	0.378	0.378	-0.022	-0.022	-0.022	8.76×10^1	-1
		7×10^4			0								
		10^5			0								
321 △		10^0	-10.07	3	6.3	0.401	0.467	0.334	0	0.022	-0.022	9.61×10^{13}	-0.9967
		10^4			4.98	1.10	1.29	0.824	0.083	0.200	0	1.96×10^5	-0.9906
		3×10^4			---	1.16	1.25	1.07	-0.023	0.065	-0.111	2.23×10^4	-0.9962
		7×10^4			2.3	0.889	1.25	0.526	-0.227	-0.118	-0.337	3.38×10^2	-0.9913
		10^5			---	2.08	3.41	1.36	-1.42	-0.722	-2.05	3.22×10^2	-0.9872
326 □		10^0	-9.71	2	6.27	0.445	0.534	0.401	0.003	0.011	0	6.15×10^{12}	-0.9982
		10^4			4.96	1.03	1.20	0.801	0.022	0.089	-0.022	1.98×10^5	-0.9949
		3×10^4			4.96	1.08	1.21	0.848	0.023	0.074	-0.022	1.21×10^5	-0.9966
		7×10^4			3.98	0.996	1.10	0.868	-0.257	0.400	-0.783	5.58×10^3	-0.9781
		10^5				1.29	1.29	1.29	-0.834	-0.834	-0.834	2.75×10^3	-1
342 ◇		10^0	-5.35	1	5.46	0.395	0.490	0.334	0	0.022	-0.022	1.26×10^{12}	-0.9954
		10^4			4.34	1.10	1.25	0.780	0.028	0.045	0	3.23×10^4	-0.9957
		3×10^4			3.94	1.09	1.25	0.913	-0.008	0.089	-0.134	1.12×10^4	-0.9947
		7×10^4			1.6	0.668	0.668	0.668	-0.067	-0.067	-0.067	8.24×10^4	-1
		10^5			1.14	0.74	0.074	0.074	-0.32	-0.32	-0.32	1.59×10^4	-1

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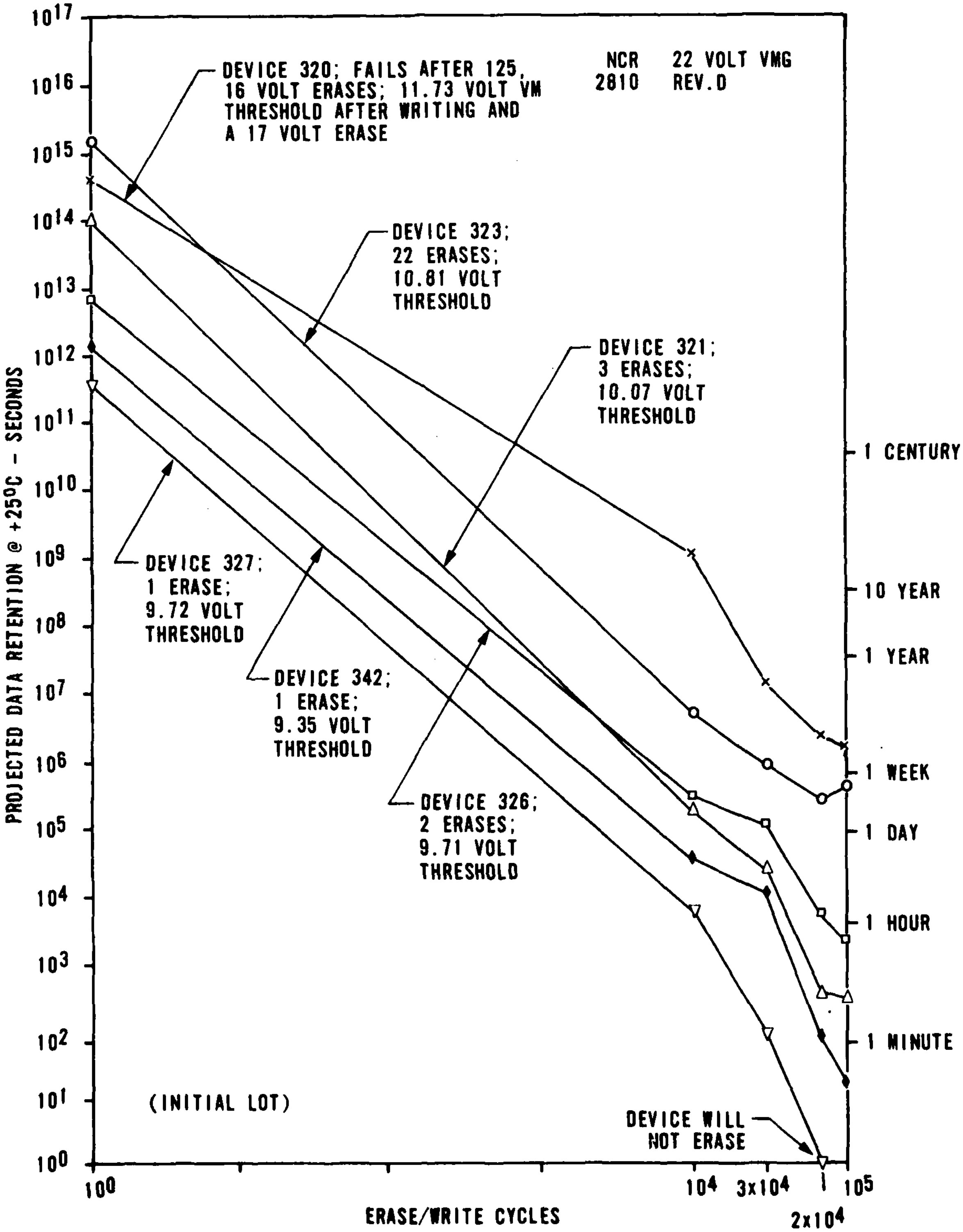


FIGURE 4-17. ENDURANCE OF NCR 2810

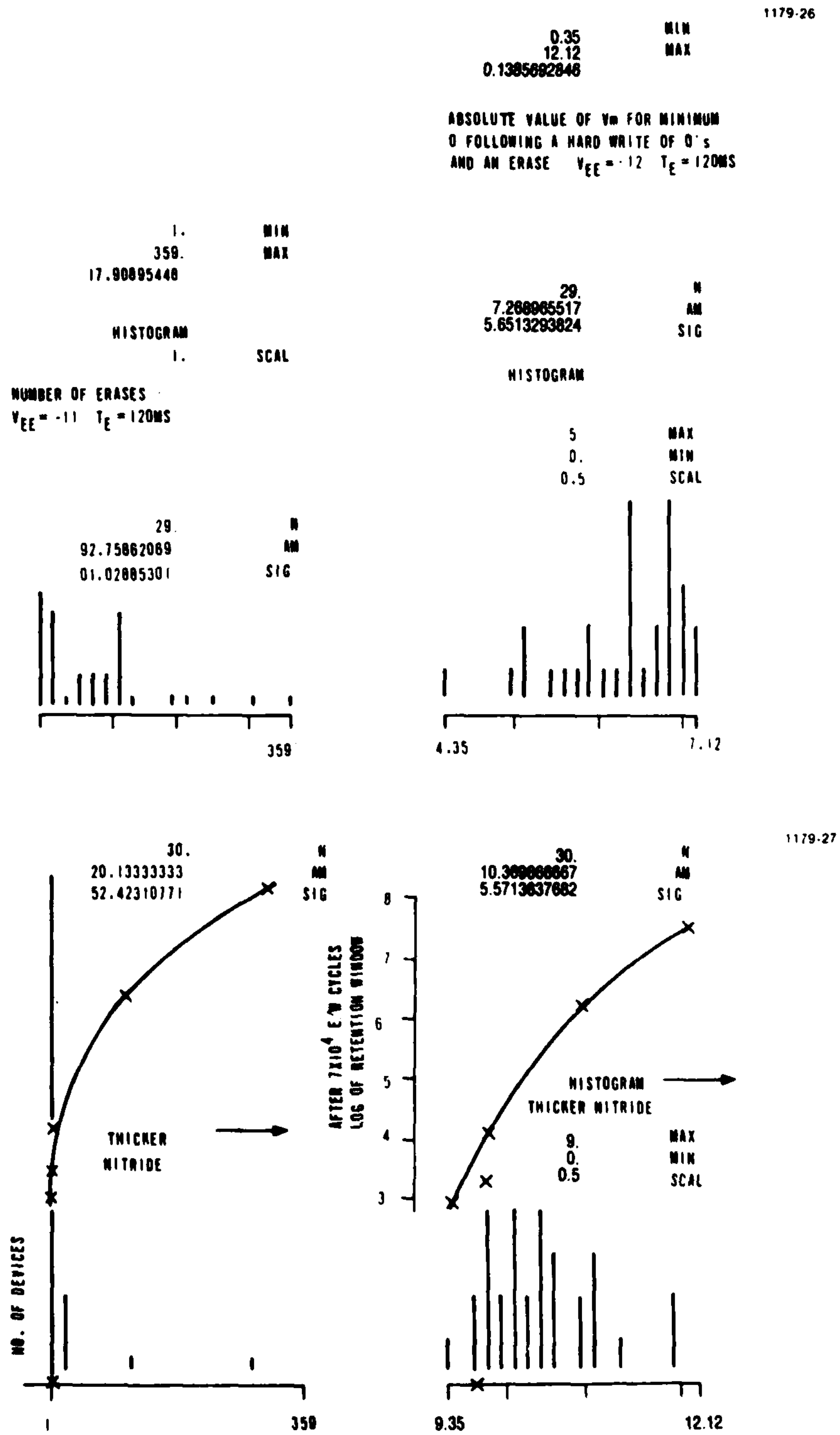


FIGURE 4-18. NCR 2810 PREDICTIVE DATA HISTOGRAM

4.6 Packaging

The ceramic Dual-in-Line side brazed packages of all devices were tested to MIL-STD-883-B, Method 5005.5, Group D tests (electrical tests waived) with the result of all devices meeting the requirements. All packages showed some degree of gold tarnishing on the package lids and leads following the salt atmosphere test.

Chip layouts for all devices are shown in the photomicrographs of Figures 4-18a, b, c, d, and e.

4.7 Conclusions

The First Interim Report concludes with an analysis of the comparative merit of each of the candidate MNOS devices based on the parameters measured and presented in that report. The conclusions showed the NCR2451/GI3400 WAROM and the NCR2810 EAROM to be optimum devices for military specification.

C7905-124

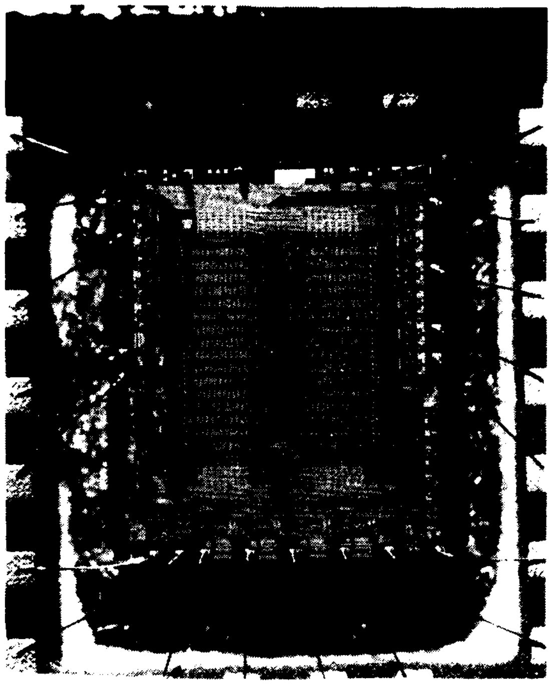


FIGURE 4-18a. NCR 2451

C7905-125

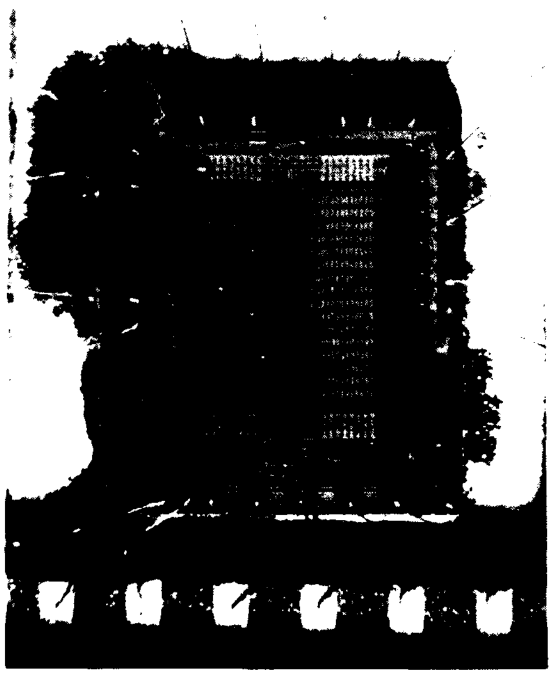


FIGURE 4-18b. GI3400

C7905-122

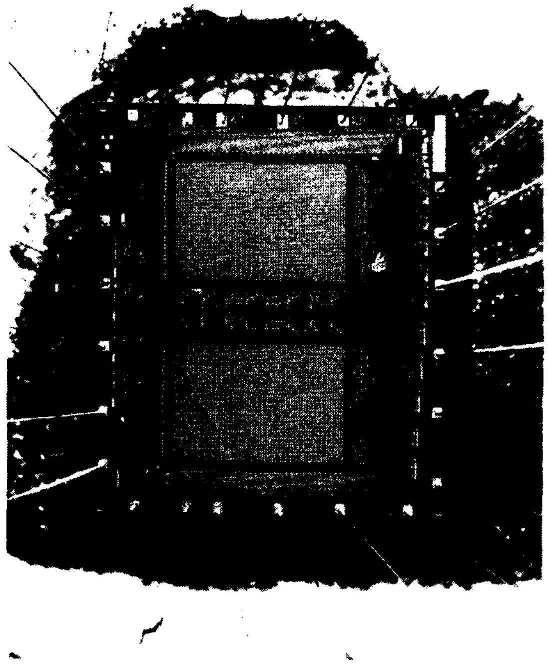


FIGURE 4-18c. NCR 2810

C7905-123

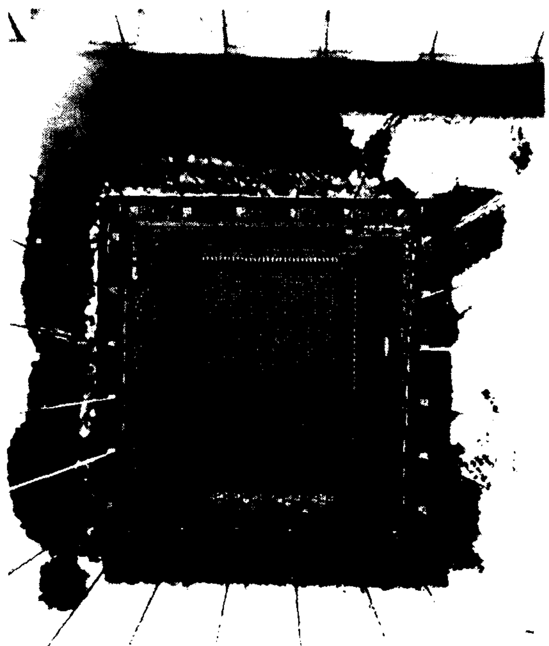


FIGURE 4-18d. GI 2401

C7908-156

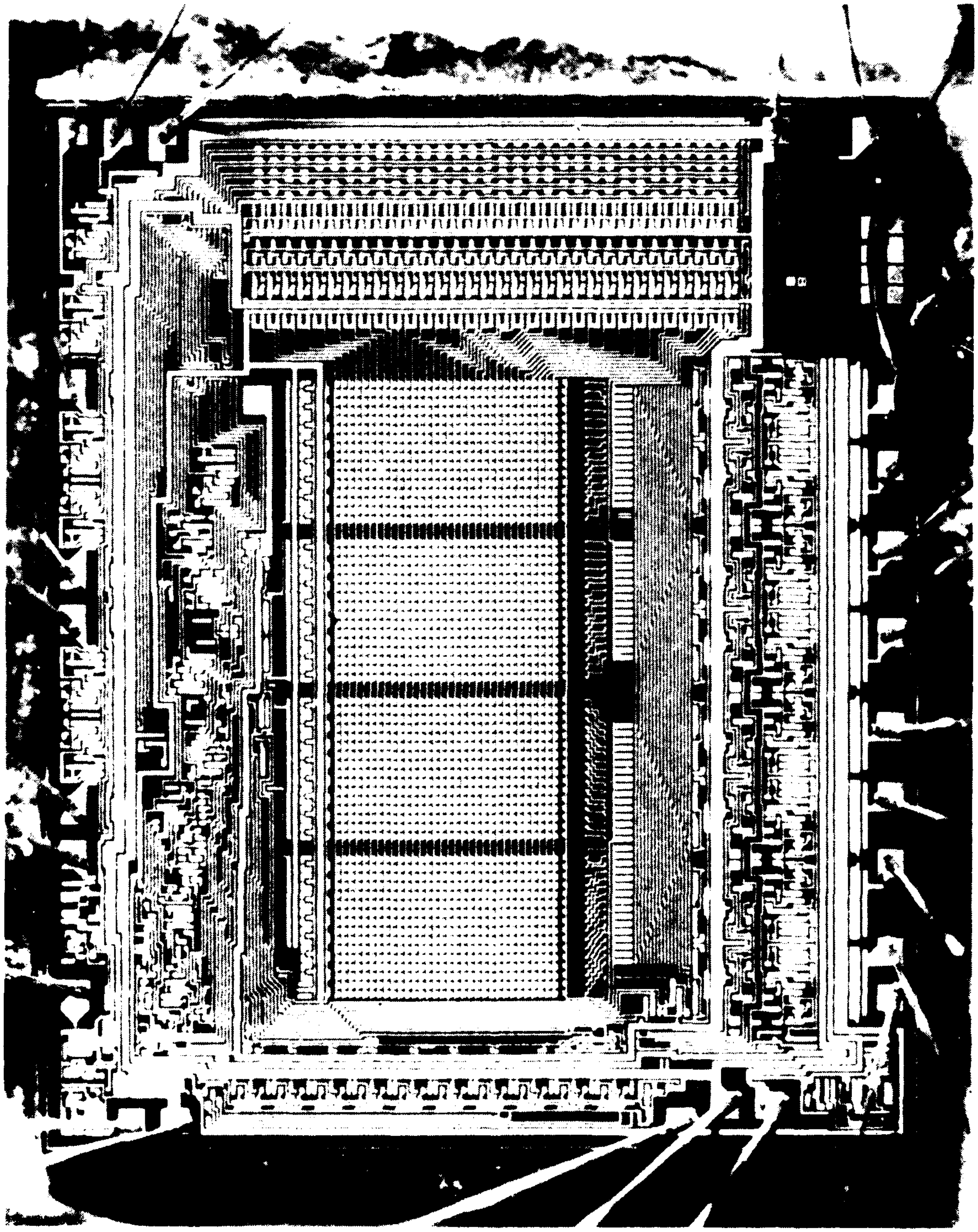


FIGURE 4-18e. NITRON 7053

5. REVIEW OF SELECTION AND CHARACTERIZATION PHASE OF THE MACI-EAROM PROGRAM

This phase of MACI completed the preselection testing and developed the parameter comparison analysis. The results of this analysis was placed in a comparison matrix. The results showed equal potential for two candidate types which resulted in an early dual approach (i.e., both NCR2810 and GI ER3400/NCR2451 types were going to be analyzed). Ordering problems with the NCR2810 (i.e., NCR was capacity limited by internal needs and GI had not yet produced the part), however, eliminated using this device in this MACI program due to lack of availability in the time frame suitable for the program.

The ER3400 devices were subjected to total dose radiation testing using CO_{60} and characterized after exposure. This was done to further clarify their applicability to military use. The results showed good performance with no data loss up to 50K RAD Si total dose.

Another question arising from military application was how well would the devices perform using shortened and reduced write and erase cycles? Could an increase in write speed be gained without significant loss in retention? Could reduced write potentials be used without significant retention loss to improve endurance performance? Characterizations of write width and write potential variations were performed and the effect on device thresholds shown. Finally, a preliminary test plan was developed for screening the ER3400/NCR2451 parts.

5.1 Background

The first four sections of the Second Interim Report showed the Introduction, Scope, Program Plan Status, and Background of the MACI-EAROM programs. Some corrections and clarifications of the first report were made. The effect of the thick oxide regions of the tri-gate MNOS memory transistor were shown as illustrated in Figure 5-1.

This figure shows that when the device is erased, the thin oxide region is written toward depletion resulting in the thick oxide regions controlling the threshold. When the charge in the thin oxide region dissipates sufficiently, it becomes the controlling threshold and the "1" threshold begins to show the normal discharge pattern characteristic of the "0" threshold (i.e., opposite slope).

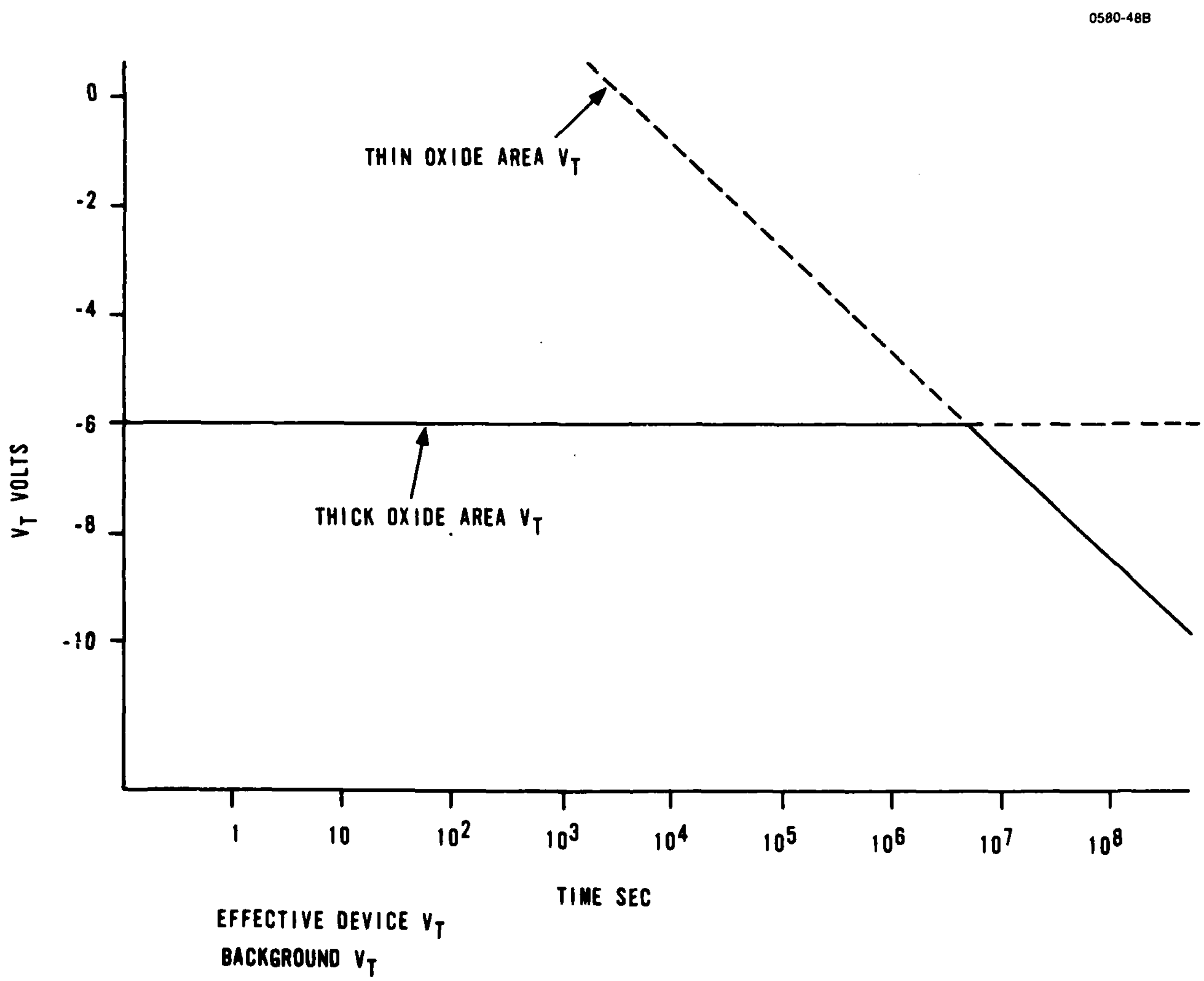


FIGURE 5-1. TRI-GATE STRUCTURE THRESHOLD EFFECT

5.2 Device Status

The First Interim Report results were discussed and device status presented at that time.

5.3 Static Electrical Tests

Devices were tested at -45°C, 0°C, +25°C, +20°C and +125°C for the following characteristics:

- Power supply current.
- Leakage currents - both I/O and erase substrate.
- Data I/O voltage levels.

Table 5-1 shows the results of these tests on ER3400's and NCR2451's. Out of 30 devices, three (3) failed one or more tests.

Figure 5-2 shows a plot of ER3400 V_{SS} supply current (I_{SS}) against temperature.

Figure 5-3 shows V_{DD} supply current (I_{DD}) for the ER3400 versus temperature in both the selected and deselected modes.

The vendor specifications on all of these devices are limited to 0 to 70°C temperature range. In order to develop the proposed slash sheet, the specifications of the dc parameters were studied to select suitable extended range values.

It was concluded that the NCR2810 showed the best results from dc electrical tests over the military range with the NCR2451 and GI ER3400 also doing well. The GI2401 and Nitron 7053 met the dc electrical tests with the latter device having the lowest performance rating of the candidate devices.

Further examination of the radiation environment performance of the 2451/3400 was performed to determine effects on device performance. Total dose appears to be the most critical parameter to MNOS devices and it was decided some investigation of this area was important from an applications viewpoint.

Some NCR2451's and GI3400's in ceramic DIPs and GI3400's in plastic DIPs were exposed to CO_{60}. The devices in ceramic DIPs failed after 5 x 10^4 RADs (Si). It was found that the devices in ceramic had older date codes in the 2451's and 3400's and the failures were attributable to marginal circuits in the device. The ER3400's in plastic packages (DIPs) operated successfully beyond 5 x 10^4 RADs (Si), as examples in Figures 5-4 and 5-5 show. The ER3400's

TABLE 5-1. DC PARAMETERS 2451/3400

DEVICE TYPE: 2451/3400

Test	Symbol	Conditions V_{SS} = 5.0V	Pins	Vendor Spec.	-45°C	0°C	25°C	70°C	125°C	Uni
Data Output High Voltage	V_{OH}	I_{OH} = -2 mA	D_0-D_3	3.5 min.	4.86	4.86	4.86	4.86	4.86	V
Data Output Low Voltage	V_{OL}	I_{OL} = 2 mA	D_0-D_3	0.4 max.	0.110	0.139	0.155	0.177	0.207	V
Control Input Leakage Current	I_{LC}	V_{IN} =-10V	C_0, C_1	-2.0 max	-.0033	-.0035	-.0041	-.0042	-.0052	µA
Data Input Leakage Current	I_{LD}	V_{IN} =-10V	D_0- D_3	-10.0 max.	-.0041	-.0045	-.0062	-.0052	-.0163	µA
V_{SS} Supply Current	I_{SS}	V_{DD} = -12V V_{GG} = -30V Chip Selected	V_{SS}	29.0 max	15.23	11.93	11.23	9.62	8.66	mA
V_{GG} Supply Current	I_{GG}	V_{DD} = -12V V_{GG} = -30V	V_{GG}	-4(2451) -3(3400)	-2.74	-2.06	-1.54	-1.50	-1.31	mA
V_{DD} Supply Current	I_{DD}	V_{DD} = -12V V_{GG} = -30V Chip Selected	V_{DD}	-25.0 max.	-19.11	-16.53	-14.01	-11.03	-8.2	mA
V_{DD} Supply Current	I_{DD}	V_{DD} = -12V V_{GG} = -30V Chip Deselected	V_{DD}	-12(2451) -7(3400)	12.04	-9.58	-8.45	-7.33	-5.97	mA

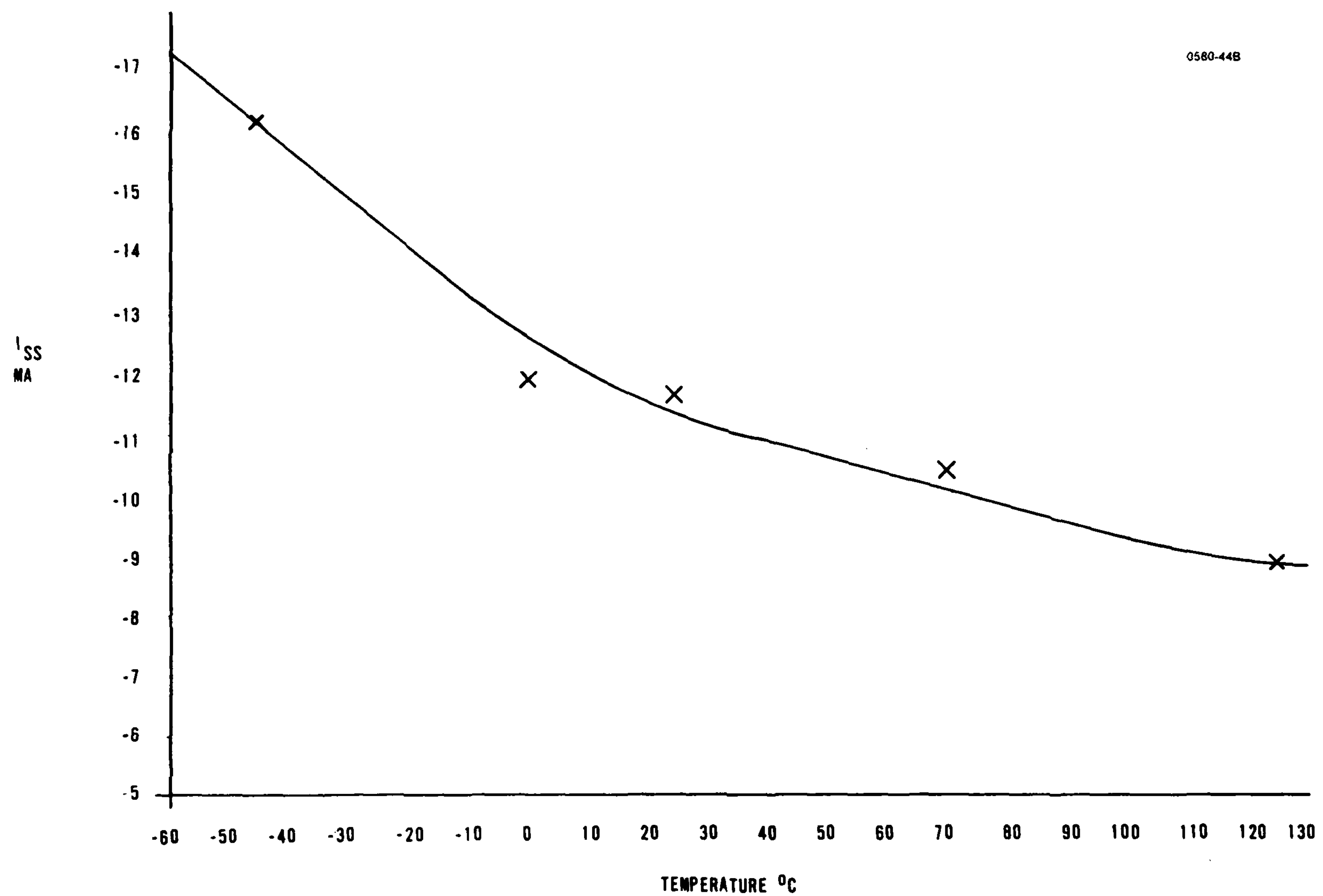


FIGURE 5-2. 3400 V_{SS} SUPPLY CURRENT (I_{SS})
VENDOR SPEC: -29 MA MAXIMUM

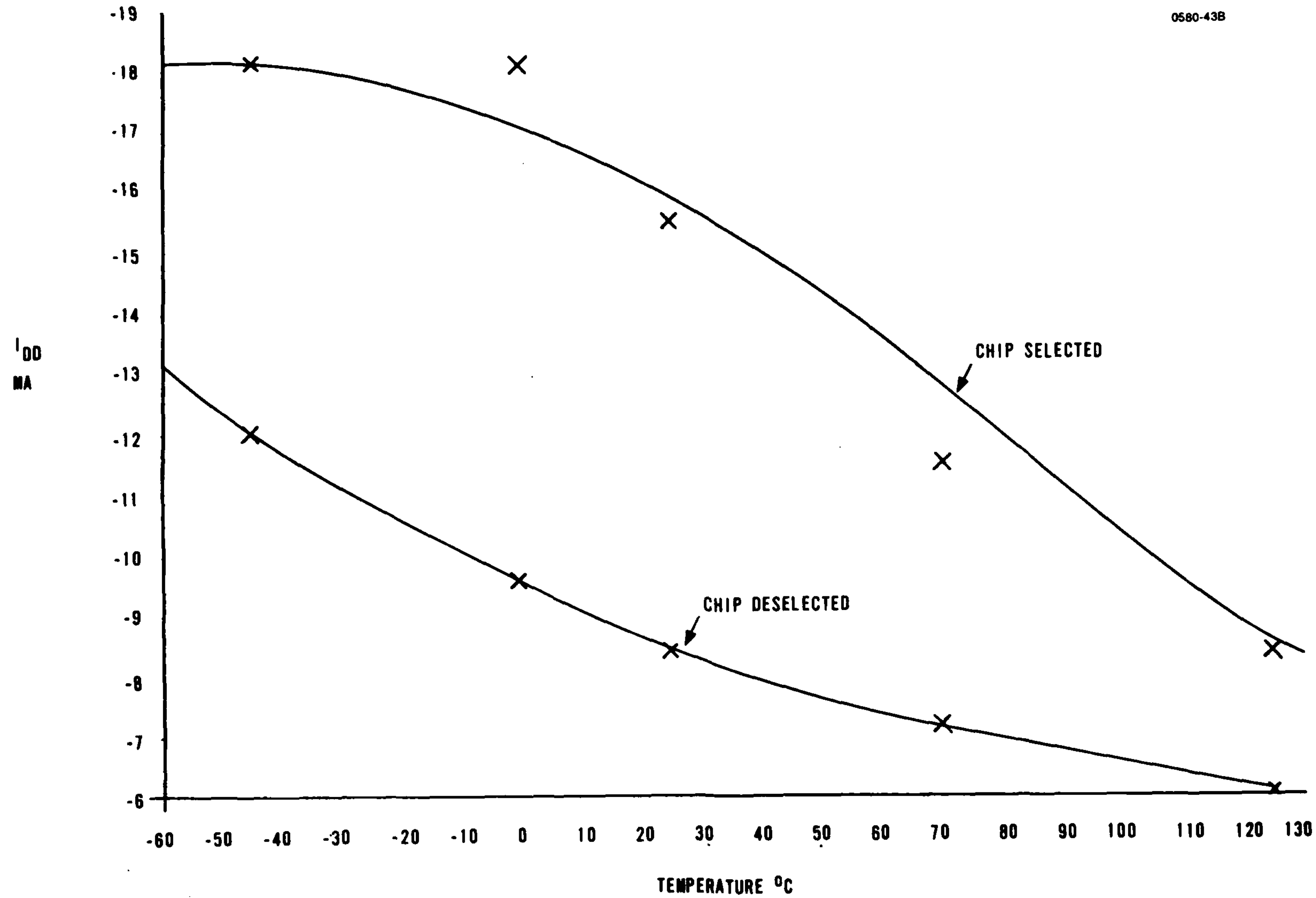


FIGURE 5-3. 3400 V_{DD} SUPPLY CURRENT (I_{DD})

VENDOR SPEC: CHIP SELECTED -25 MA
CHIP DESELECTED -12 MA

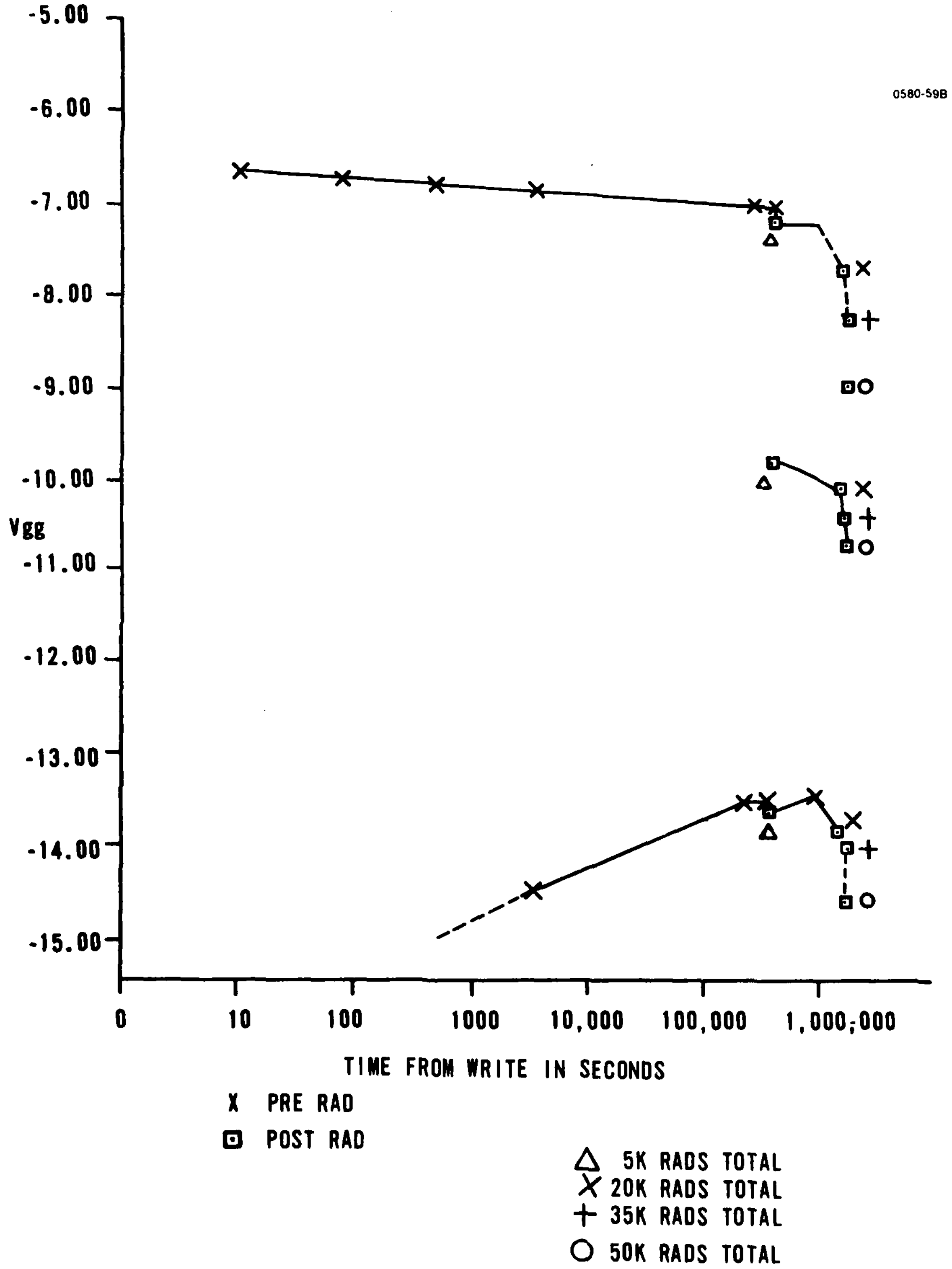


FIGURE 5-4. V_T VERSUS TOTAL DOSE 3400 NO. 3

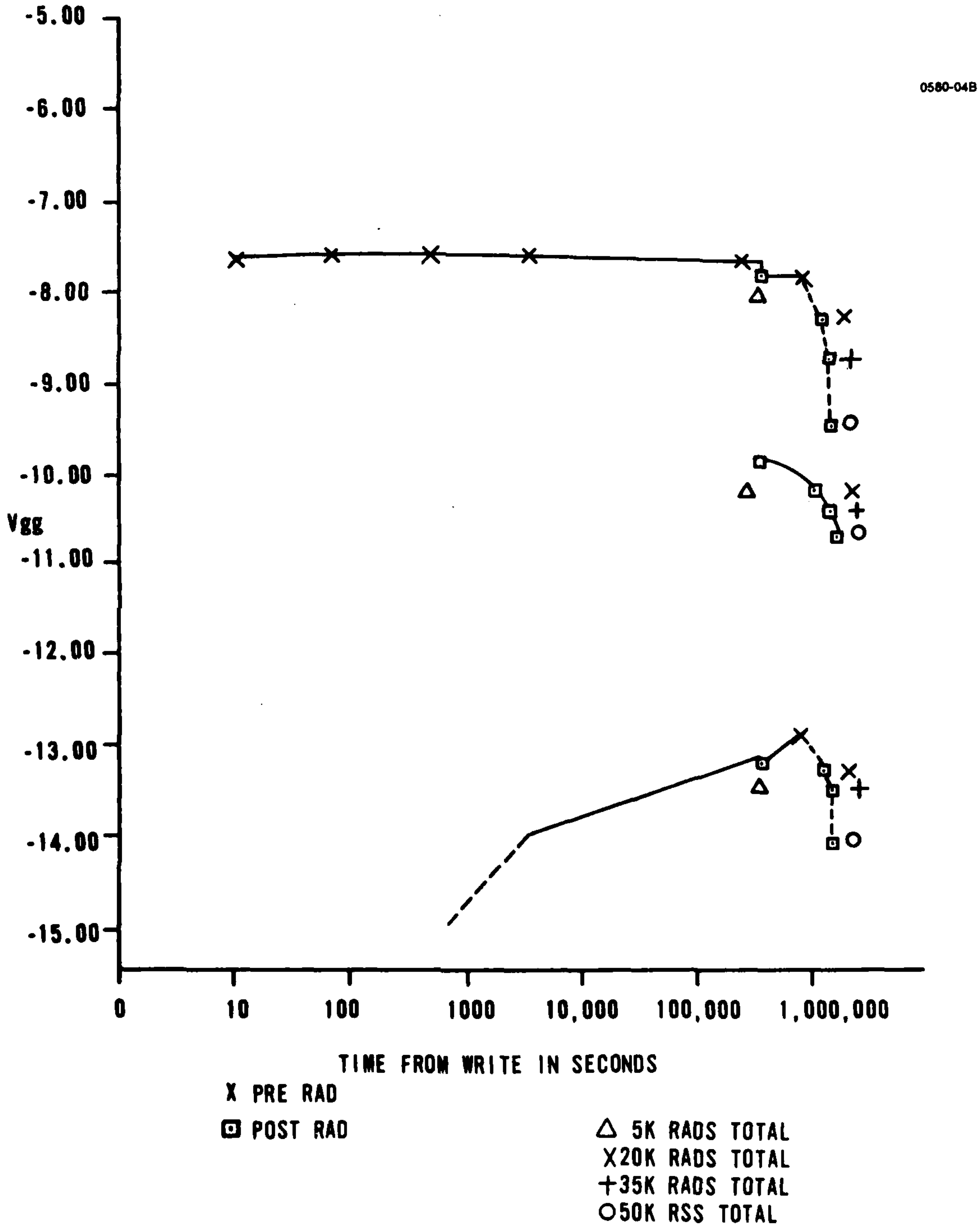


FIGURE 5-5. TOTAL DOSE VERSUS V_T

were erased and written and allowed to stand for 2 x 10^5 seconds to simulate in-system conditions. The devices were then exposed to succeeding doses of radiation as shown, after which the "1" and "0" thresholds and reference voltage of each device were measured and functional reads were performed. The results in Figures 5-4 and 5-5 show the negative voltage shift in both "1" and "0" thresholds and the reference window. It is notable that the threshold window (Vt "1" to "0") remains approximately the same as pre-rad. The reference voltage against which each threshold is compared by the sense amplifier also shifts in the same direction under radiation exposure, thus, causing the predicted retention to remain the same. In some of the NCR 2451's, the reference voltage went positive with increasing radiation, which would tend to significantly shorten data retention time.

Read access schmoo diagrams were developed for the irradiated devices to determine the functional affect of the radiation upon the devices. Figures 5-6 and 5-7 show schmoo's run at +25°C and +85°C on a 3400 after irradiation. It can be seen that this device meets the specified access time at both temperatures after irradiation. Comparison to Figure 5-8, which shows a schmoo of a non-radiated control device, illustrates the degradation in performance due to irradiation. It can be concluded that the ER3400 devices can operate in the military environment after exposure to 50K RADs of radiation as long as the proper margins are allowed in device timing. It also shows that MNOS devices can retain data under moderate radiation conditions.

5.4 Writing Conditions

In data acquisition applications, MNOS devices that have fast write times and high endurance characteristics would be optimum. The question then arises; can the write cycle be reduced and/or the write bias be changed on the standard EAROMs/WAROMs to match these conditions? In order to provide some insight into these applications, tests were developed on the relationship of the write cycle width and the voltage threshold, and the write bias level and the threshold voltage.

Figure 5-9 shows a composite graph of the number of write pulses used to write the device plotted against the resulting memory threshold voltage. Composite graphs are drawn by varying the width of the pulses. This device happens to be a NCR2810 that was measured to have a relatively thin nitride and exhibits significant Vt shifts when the wider width pulses are used near the maximum number of pulses. Figure 5-10 is a similar graph of a relatively thick nitride part which does not exhibit these abrupt changes in the region tested. It can be seen in both graphs that the Vt change is saturating at the maximum widths tested which represents only 1/100th of the specified value of write width.

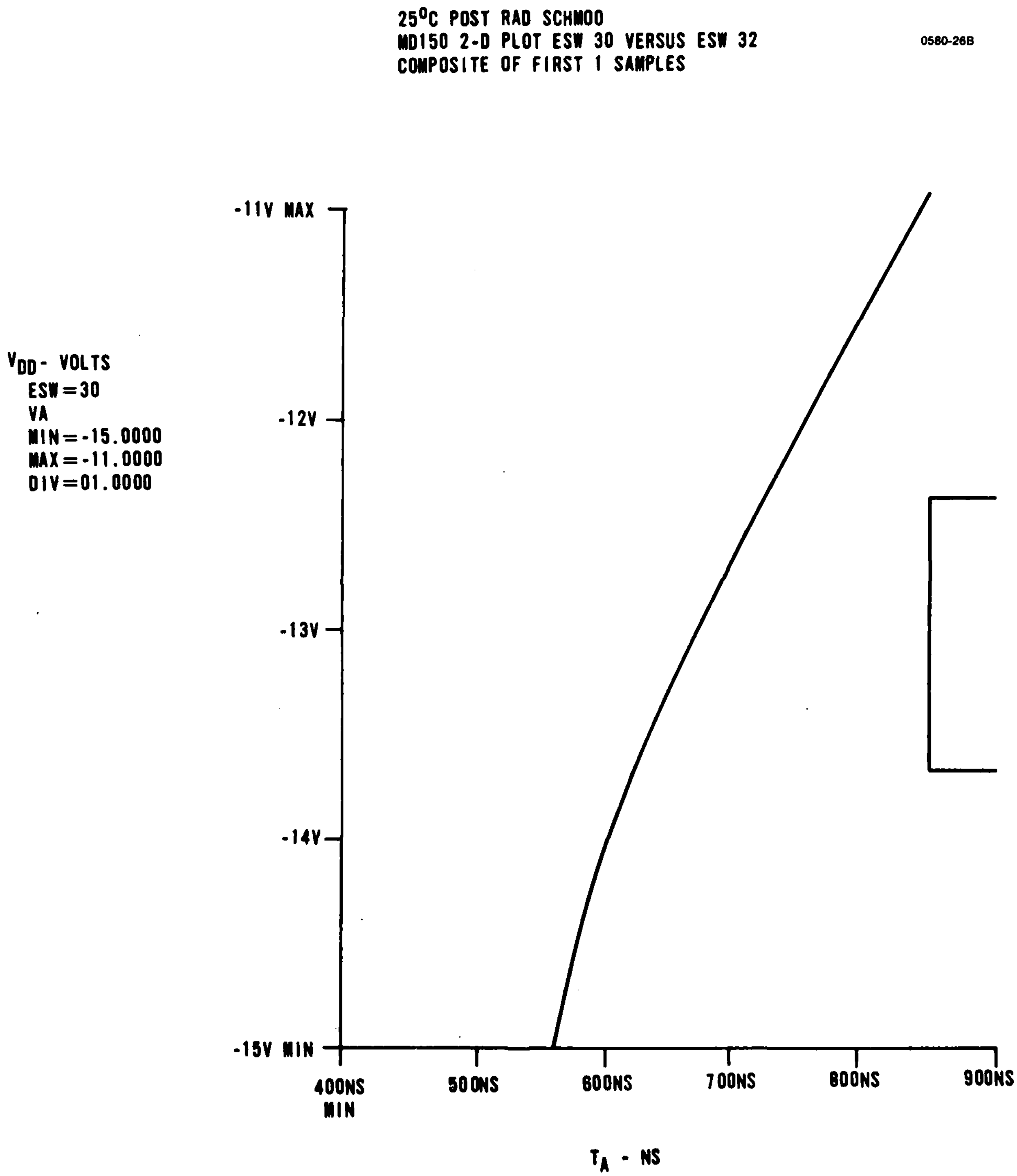


FIGURE 5-6. 3400 NO.3 25°C POST RAD SCHMOO

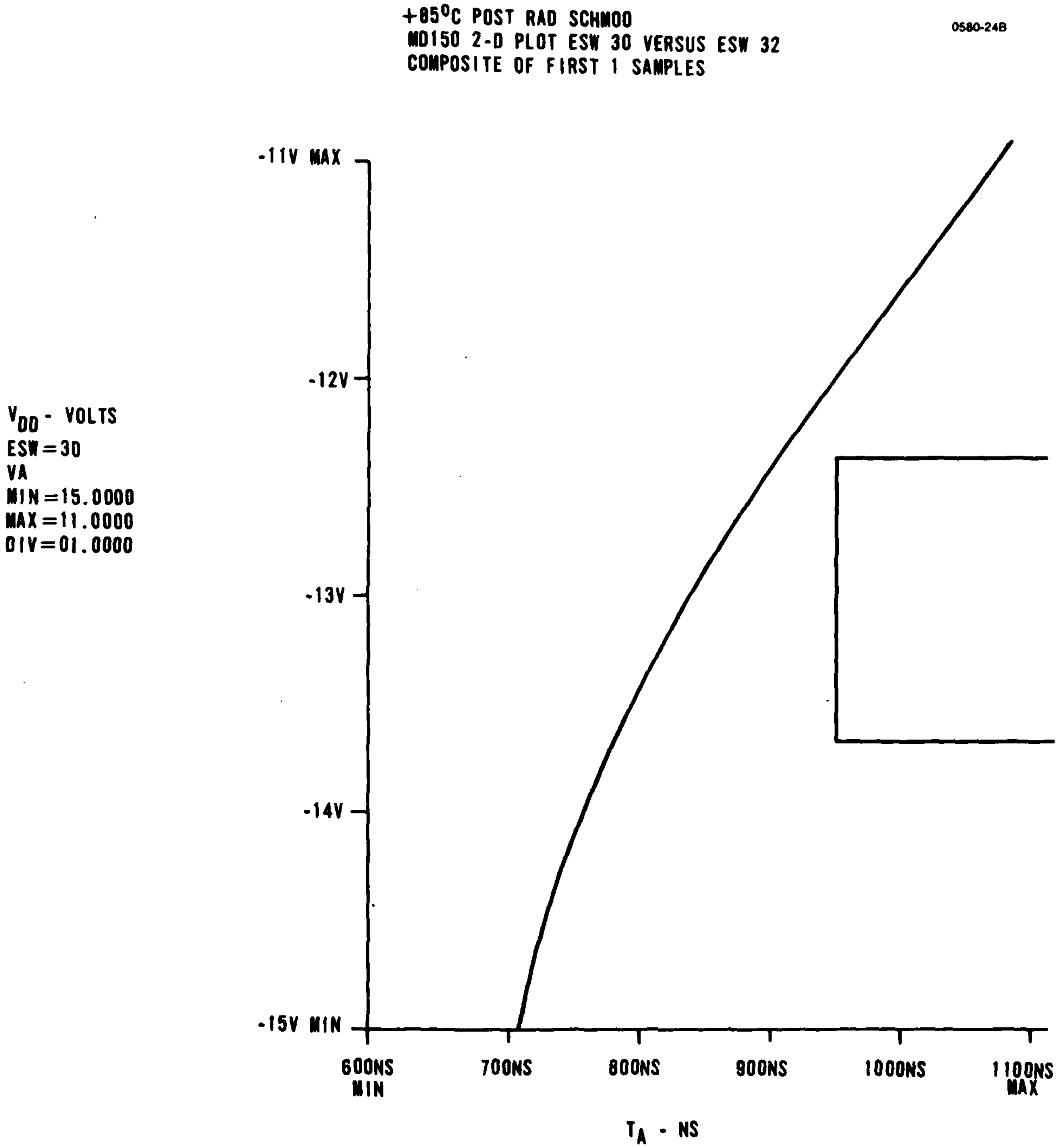


FIGURE 5-7. ER 3400 NO.3 +85°C POST RAD SCHMOO

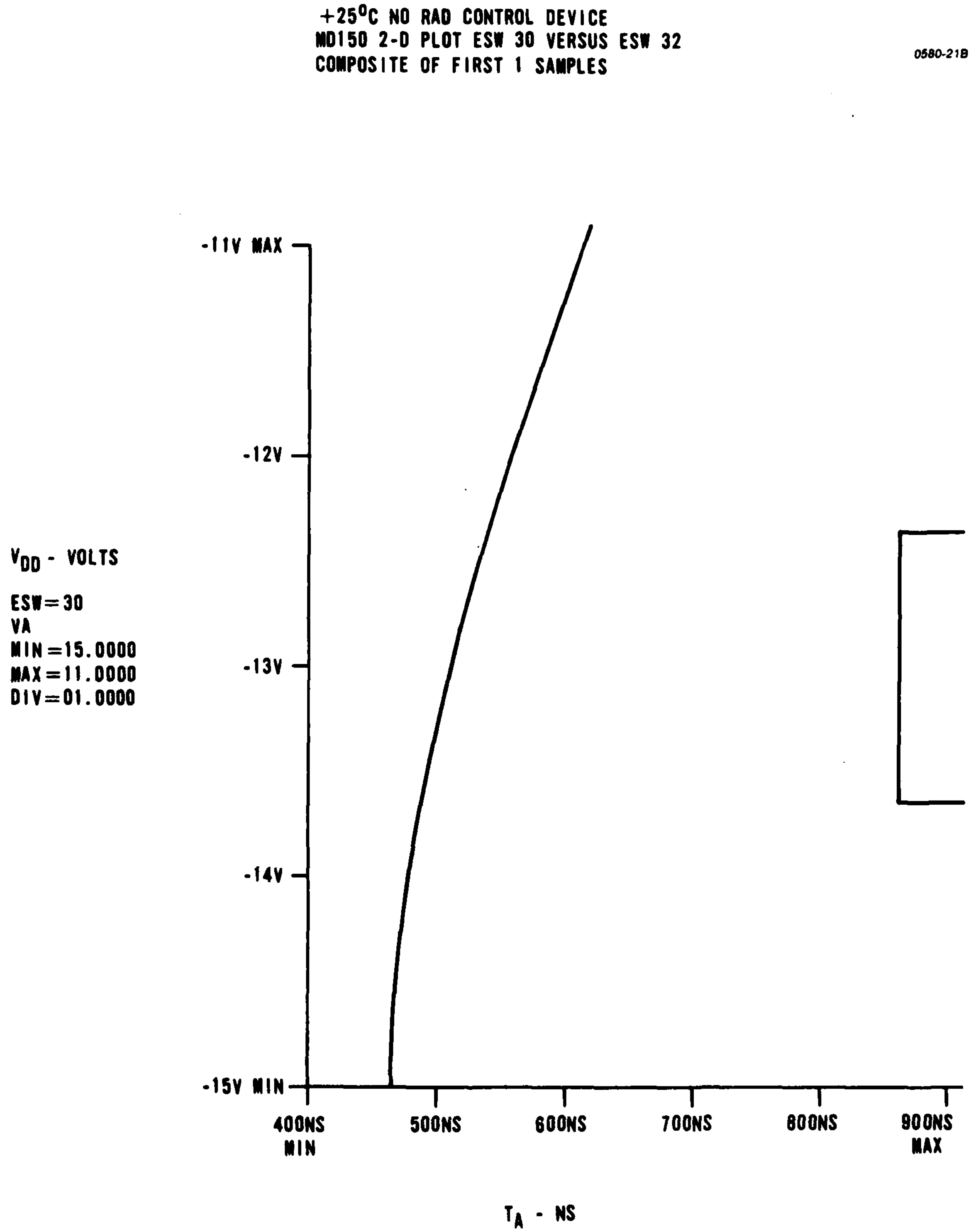
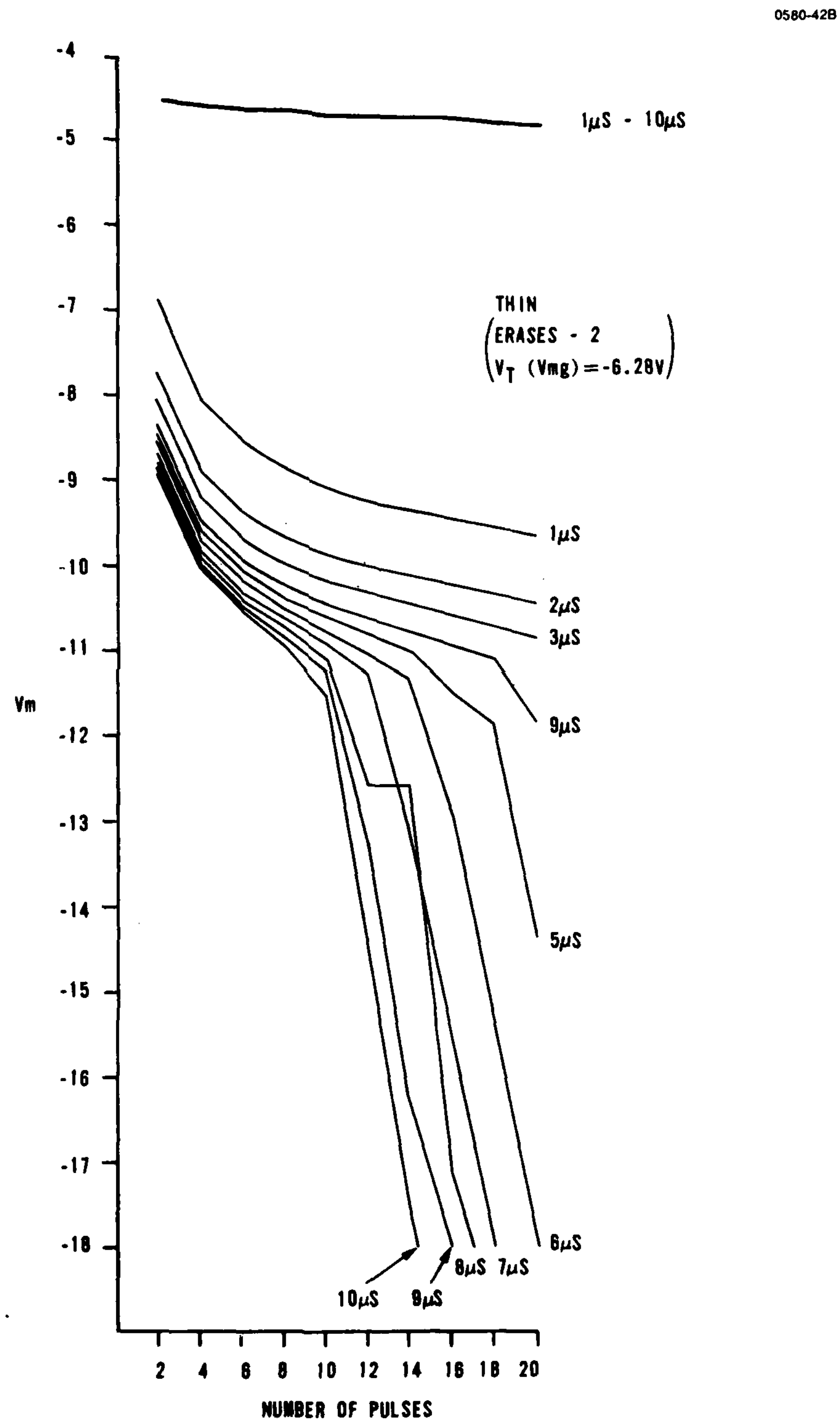
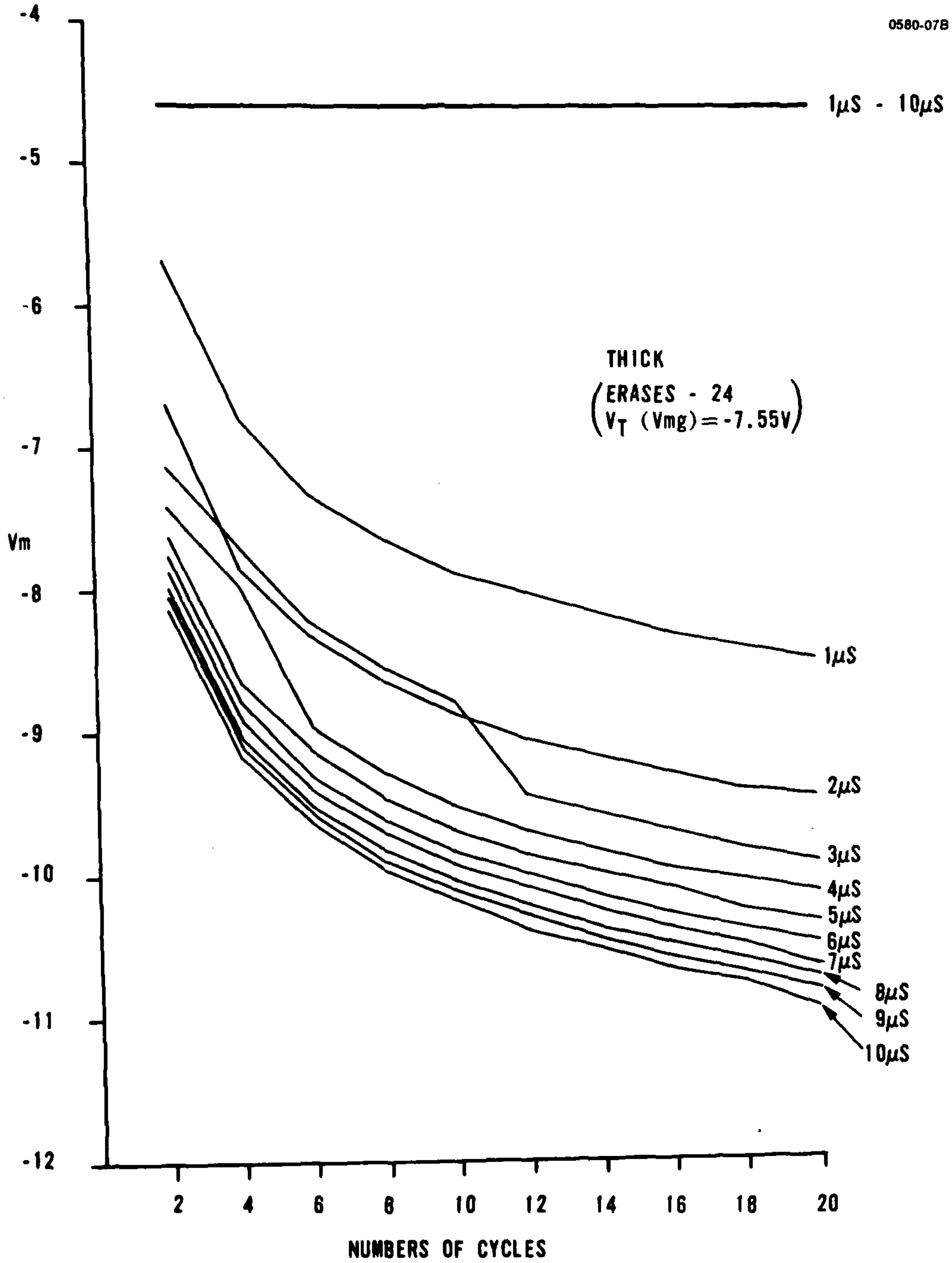


FIGURE 5-8. 3400 NO. 26 +25°C NO RAD CONTROL DEVICE



(THIN NITRIDE PART - 2 ERASES V_T (VMG)=6.28V

FIGURE 5-9. WRITE WIDTH VERSUS V_T 2810 NO. 318



("THICK" NITRIDE PART - 24 ERASES VMG -7.55V)

FIGURE 5-10. WRITE WIDTH VERSUS V_T 2810 NO. 328

The other method of increasing endurance is to reduce the write potential. Tests were run varying the write potential and using the specified width. Figure 5-11 shows a plot of the write potential versus the resulting memory transistor threshold. For the device shown (relatively thick nitride), saturation occurs at approximately -18 volts, resulting in a relatively shallow threshold of -9 volts. Figure 5-12 shows a similar plot of a relatively "thin" nitride device. This indicates that saturation does not occur out to -22 volt writes and the resulting threshold is deeper (i.e., -10.5 at 22V writes) than the earlier part.

The WAROM devices could not be tested for write voltage variation due to the internal switching circuit arrangement. These devices were tested for write width variation. Figure 5-13 shows a plot of the threshold versus write width characteristics of a "thick nitride" NCR2451. In comparison, Figure 5-14 is a similar plot of a "thin" nitride part. It can be seen that the thin nitride part writes faster into saturation than it's thicker nitride cousin. Saturation is roughly achieved at 200 μs write width for the thinner nitride part while it takes approximately 500 μs for the other part.

It can be determined from this data that:

- Most write specifications are extremely conservative and may therefore contribute to the low endurance performance.
- "Thin" nitride parts appear to write faster with deeper thresholds resulting.
- Devices that are endurance stressed write faster and appear to have deeper Vt than virgin parts.
- Faster write times could be used in data acquisition applications with little apparent retention loss.
- Reduced write voltage is feasible in devices not restricted by circuit organization as a method of enhancing endurance.

5.5 Comparison Matrix

Table 5-2 shows a direct comparison of all candidate devices used in the MACI program. Twenty-two different parameters are compared with the results indicating the NCR2810 and NCR2451/GI ER3400 as being the best candidates for final device selection.

Problems encountered in procuring the NCR2810 at this phase (due to capacity limitations at NCR and GI or Nitron not yet being in production) eliminated it from the final selection since test schedules for MACI program milestones could not be met. The NCR2451/GI ER3400 then became the device type selected for proposed qualification and further use in the final phase of MACI.

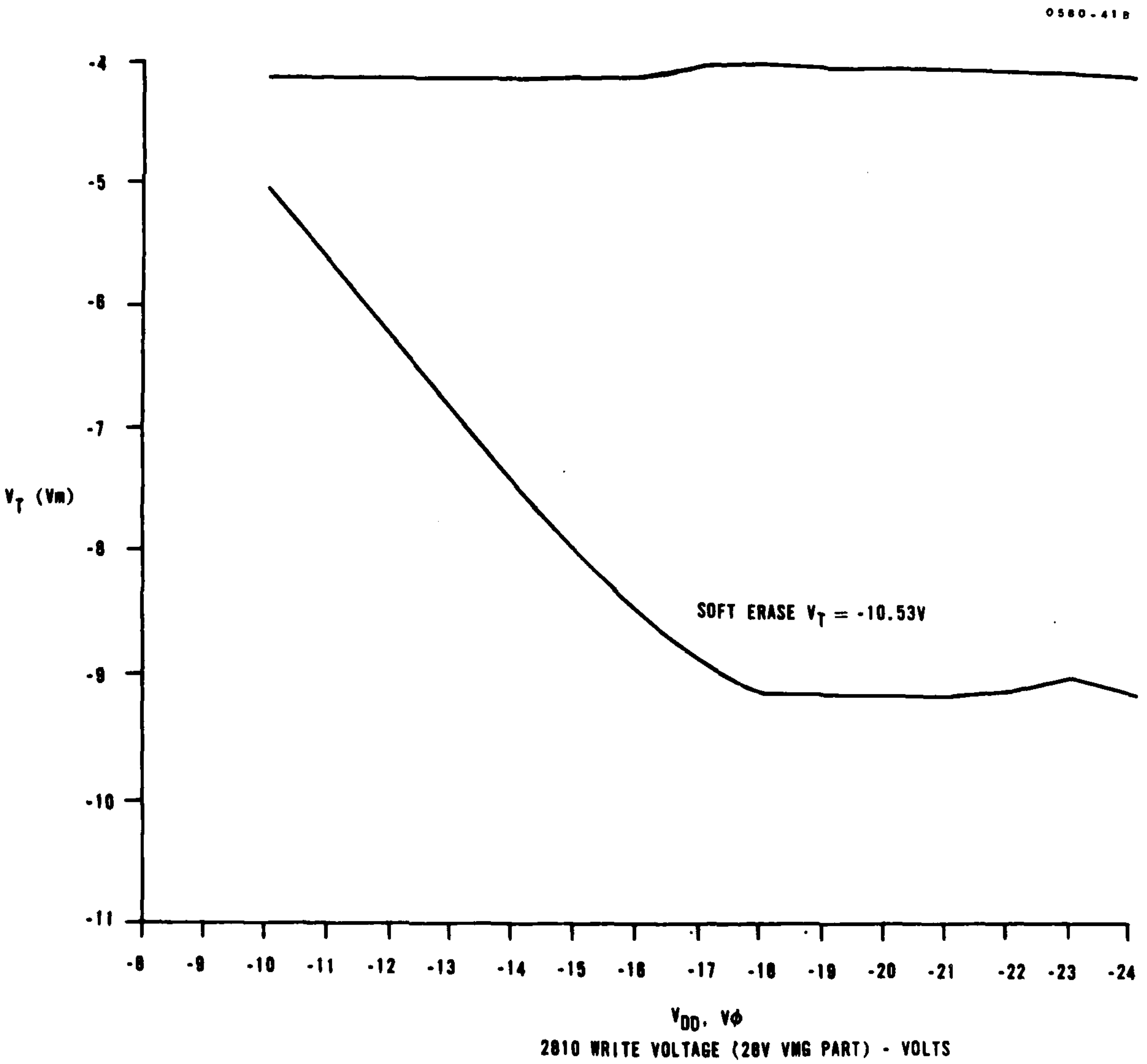


FIGURE 5-11. WRITE VOLTAGE VERSUS V_T
(THICK NITRIDE PART)

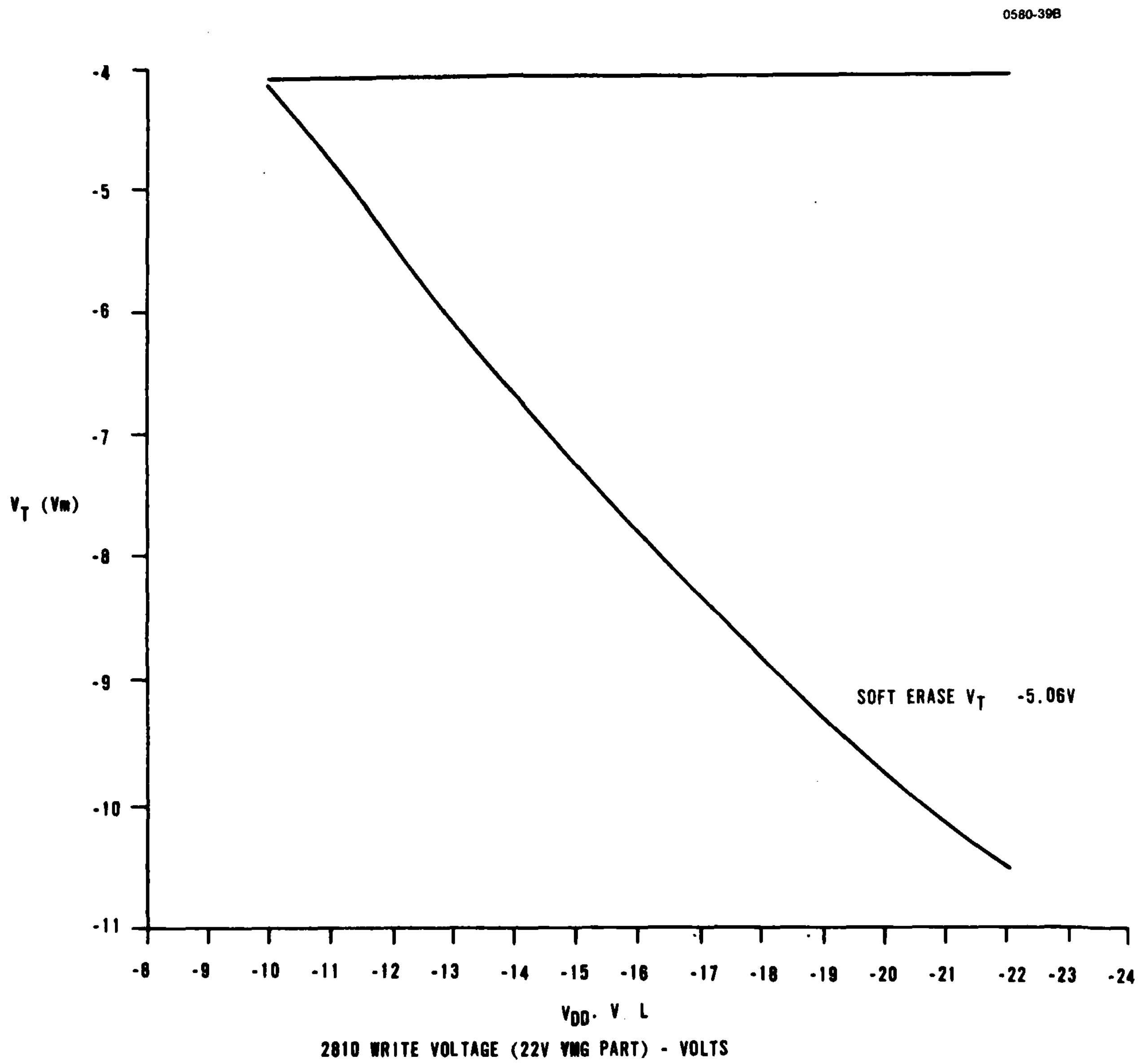


FIGURE 5-12. WRITE VOLTAGE VERSUS V_T
(THIN NITRIDE PART)

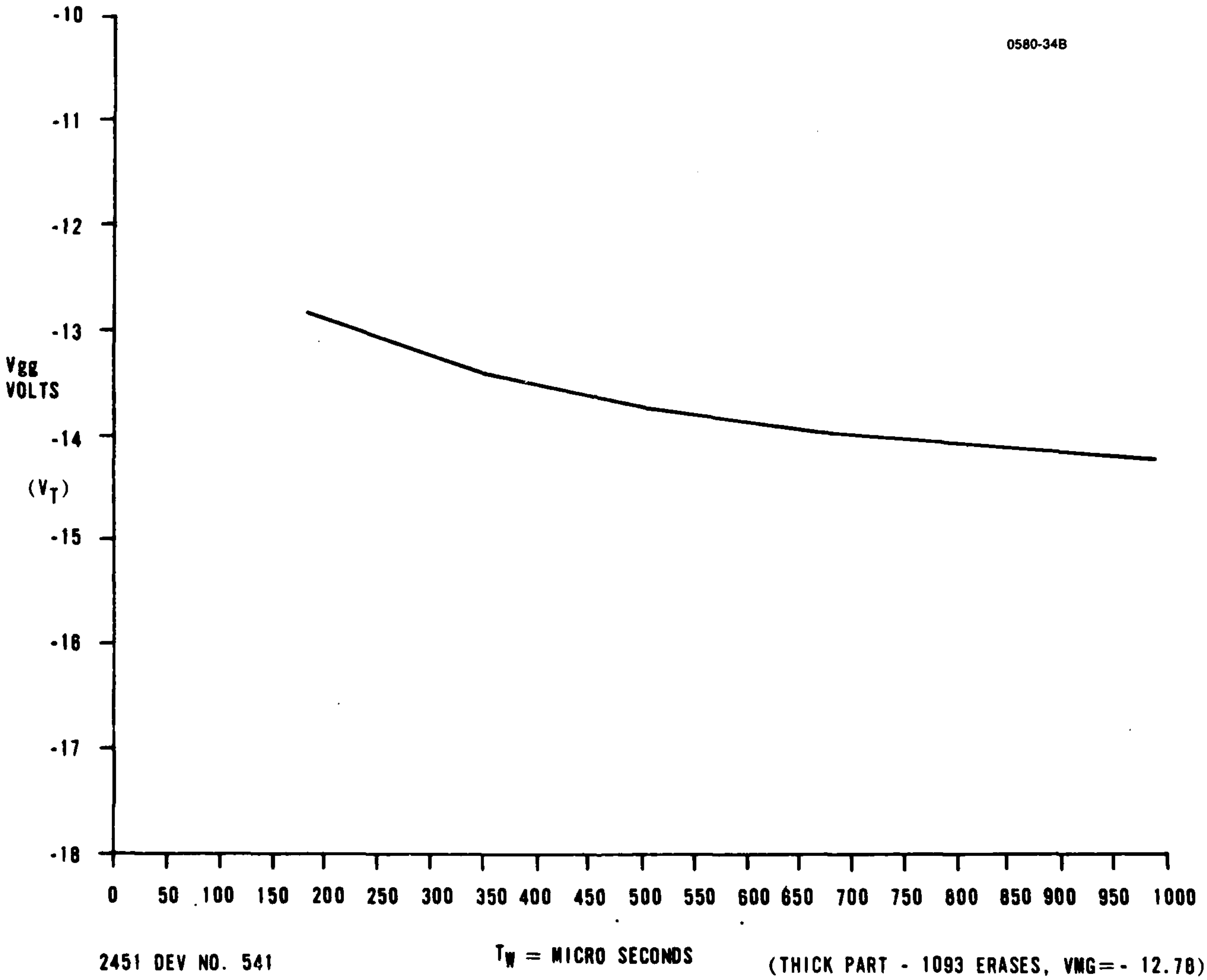


FIGURE 5-13. WRITE WIDTH VERSUS V_T 2451 NO. 541

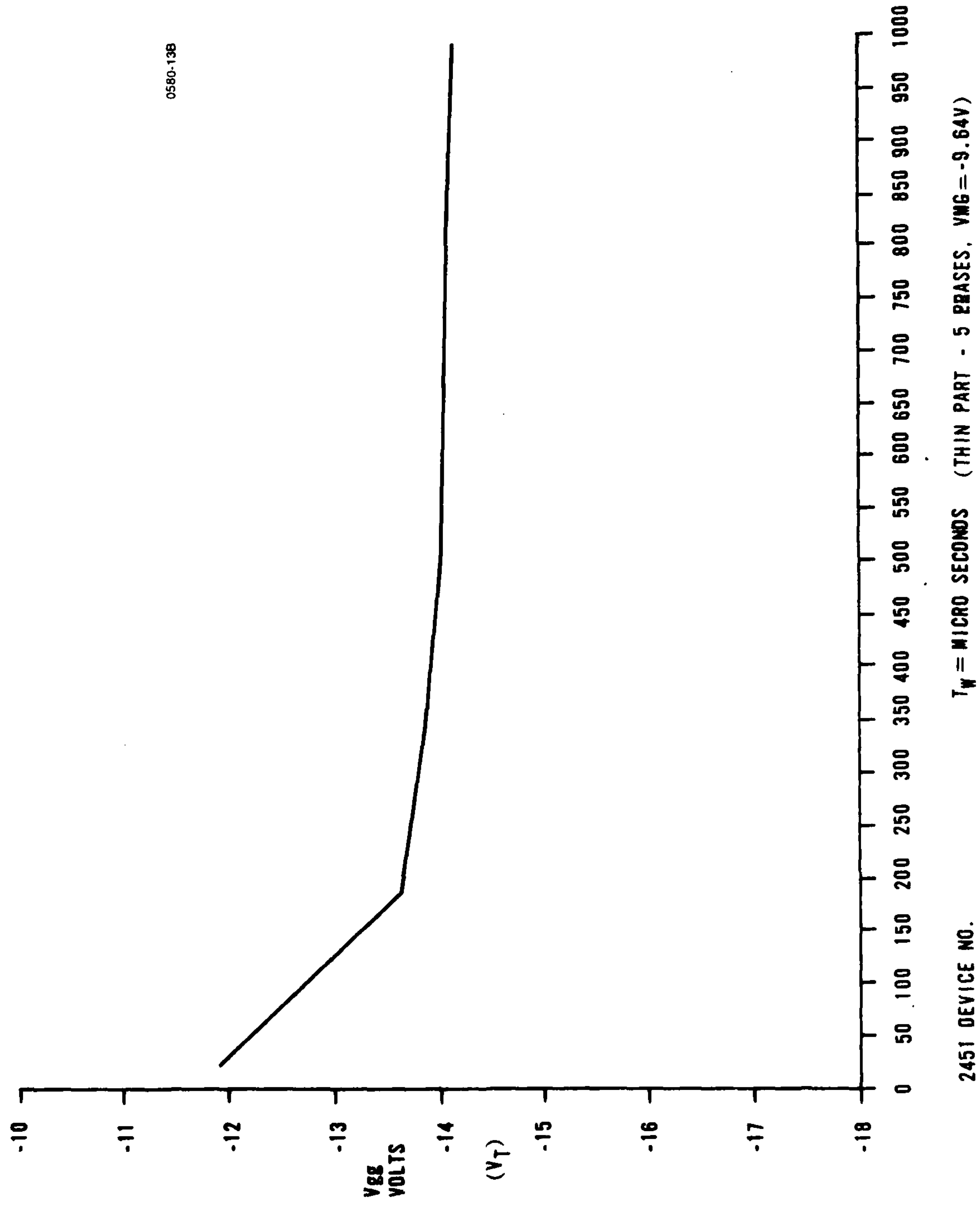


FIGURE 5-14. WRITE WIDTH VERSUS V_T 2451 NO. 509

TABLE 5-2. MNOS DEVICE COMPARISON TABLE

DEVICE TYPE	COMPAT. DEVICES	MILITARY APPL. COST @10K PCS $Bits/Word	MILITARY APPL. DENSITY SPEED/TACC -55 +125°	RETENTION Static 25°C STATIC +125°	RETENTION BIASED Static +25°C READ DISTURB Scale 1-4	ENDURANCE RETENTION AFTER 10^4 E/W	VENDOR SUPPORT	POWER MW +25 -55	POWER MW +125 WRITE	DC PARAMETERS GRADED 1 - 5	RADIATION ΔV_T @2K RADS	PACKAGING	V_T READ	COMMENTS
WAROM NCR2451 NCR 1K x 4	NC7451 ER3400	0.3¢/Bit	4K Bits	1.7×10^{10} - 4×10^{10} Sec	8.3×10^8 - 1.7×10^9 Sec	6.5×10^5 to 1.6×10^7	STRONG > 5 YRS	325	260	3	0.28 V	22 PIN CER DIP	YES	Good Performer Fast Second source available
		4	.35μs-.65μs	1.7×10^7 - 1.7×10^8	3			393	227					
ER3400 GI WAROM 1K x 4	NC7451 NCR2451	0.35¢/Bit	4K Bits	1.1×10^{10} - 1.1×10^{11} Sec	No Test	3.2×10^6 to 3.86×10^8	STRONG > 5 YRS	339	283	3	0.18 V	22 PIN CER DIP	YES	Good Performer Fast Second source available
		4	.3μs - .6μs	1×10^8 - 3×10^8 Sec	2			428.5	270					
ER2401 EAROM 1K x 4 GI	NCR2401	0.15¢/Bit	4K	1×10^{18} - 4.7×10^{18} Sec	2×10^{20} - 9.5×10^{21} Sec	1×10^8 to 1×10^{12}	WEAK < 3 YRS	152	114	2	0.033 V	24 PIN CER DIP	YES	No vendor support Slow
		4	.8μs-1.5μs	4.5×10^{12} - 1×10^{17} Sec	4			228	638					
NCR2810 NCR 2K x 4 EAROM	ER2810 NC2810	0.1¢/Bit	8K	2×10^{12} - 2×10^{14} Sec	2×10^{12} - 7×10^{14} Sec	2.5×10^5 to 3.7×10^{11}	STRONG > 5 YRS	190	114	1	0.08 V	24 PIN CER DIP	YES	Best all-around performer Hi-density
		4	.7μs-1.0μs	4.4×10^9 - 1×10^{11} Sec	1			266	638					
NC7053 128 x 8 Nitron WAROM		1.3¢/Bit	1K	No Test	No Test	No Test	UNKNOWN (new design in works)	416	307	5	No Test	No Test	NO	Poor high temperature Performance not available
		8	1.5μs-2.7μs	No Test	No Test			527	No Test					

6.0 REVIEW OF SCREEN TESTING AND SLASH SHEET DEVELOPMENT PHASE OF MACI PROGRAM

This phase of the MACI program started with the finalization of the test plan and the beginning of the screening procedure. After some initial problems regarding the decision to use one or two device types as the final candidate, the NCR2451/GI ER3400 device was chosen for further testing. While the NCR2810 had many favorable characteristics to indicate its suitability for military use, and though some were ordered for screening, the lack of availability at that time eliminated their use in the rest of the program.

The NCR2451 and GI ER3400 were then started into screening. By maintaining an accurate log on how many, where, and what type of device failures occured, an indication of screening yield for potential users was developed. The five different test categories each device was subjected to are listed below:

- Preconditioning or leak tests.
- Functional screen tested over military temperature range.
- Burn-in and retention.
- DC parameter tests.
- Final functional.

Fifty devices passing all these tests were delivered to ERADCOM. Other devices had life tests performed to determine lot viability.

Methods of accelerated and predictive testing of time associated parameters of MNOS devices were discussed in detail. A predictive retention testing method of using a nomograph developed for the MACI program was shown with an example case. The data developed during the early phases of MACI was used to develop a graph of the relationship between the "soft erase threshold" and the endurance. From this graph new device measurements were plotted and the retention after 10^5 erase/cycles predicted. The relationship to the erase substrate leakage of the soft erase threshold was then shown. This work indicated that endurance prediction could be performed using any of the following methods depending upon which was more suitable to the particular device:

- Measurement of "soft erase" thresholds.
- Measurement of erase substrate leakage.
- Measurement of the number of soft erases until data change.

Testing to produce a useful read disturb prediction method was performed. While the results were inconclusive due to the small sample size and long delays needed to verify results, some indication of a positive correlation was developed.

6.1 Test Plan

The final test plan which was largely developed in the previous phase was refined and finalized with improved procedures and a modified burn-in circuit arrangement. The modified circuit insured that voltage transients due to power outages would not cause an improper voltage sequencing to which the NCR2451/ER3400 is sensitive.

6.2 Screen Test Results

One-hundred-sixty devices were screened starting with the leak tests shown below:

- Stabilization bake - Method 1008.1, Cond C.
- Temperature cycling - Method 1010.2, Cond C.
- Constant acceleration - Method 2001, Cond E only.
- Seal - Fine
Gross
Serialization soak at +125°C.

One-hundred-forty devices passed this test. Figure 6-1 shows the breakdown of where devices failed in the screen testing. The tests where most devices failed are shown to be the full military range functional tests and the 160-hour retention tests. In the functional tests the NCR2451 tended to fail at low temperatures (≤-40°C) by not functioning (i.e., loss of write erase or read function). ER3400's, on the other hand, tended to malfunction at high temperatures (i.e., ≥+100°C).

In the retention tests the ER3400 showed excessive rate of charge loss (i.e., rate of threshold decay) in over 50 percent of the initial devices tested. Figure 6-2 shows a distribution of the +125°C rate of threshold decay for both NCR2451's and ER3400's. This characteristic is much more severe for most ER3400 devices than that of the 2451's. Earlier ER3400's did not show this characteristic. Some indication of a relationship of a switch to LPCVD nitride may be suspect. New ER2810's made by GI do not appear to have the same problem and these parts are also made with LPCVD nitride. By performing second measurements of +125°C retention on many of the parts (ER3400's) failing the initial tests, the discharge rates on approximately 40 percent of the parts improved significantly. This indicated permanent device threshold shift occurring during the initial burn-in period was not related to retention.

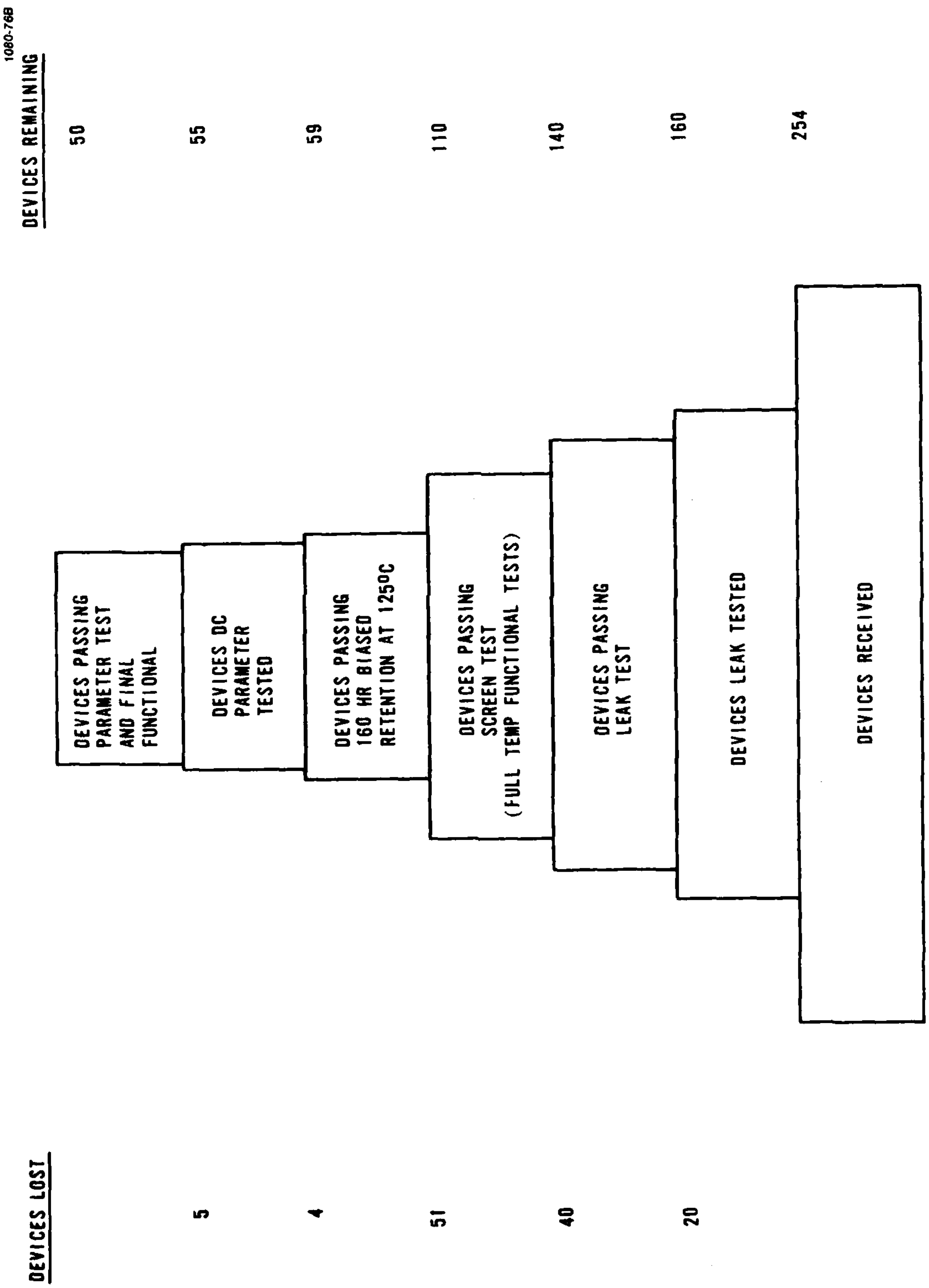


FIGURE 6-1. SCREEN TEST YIELD FOR NCR 2451/ER3400

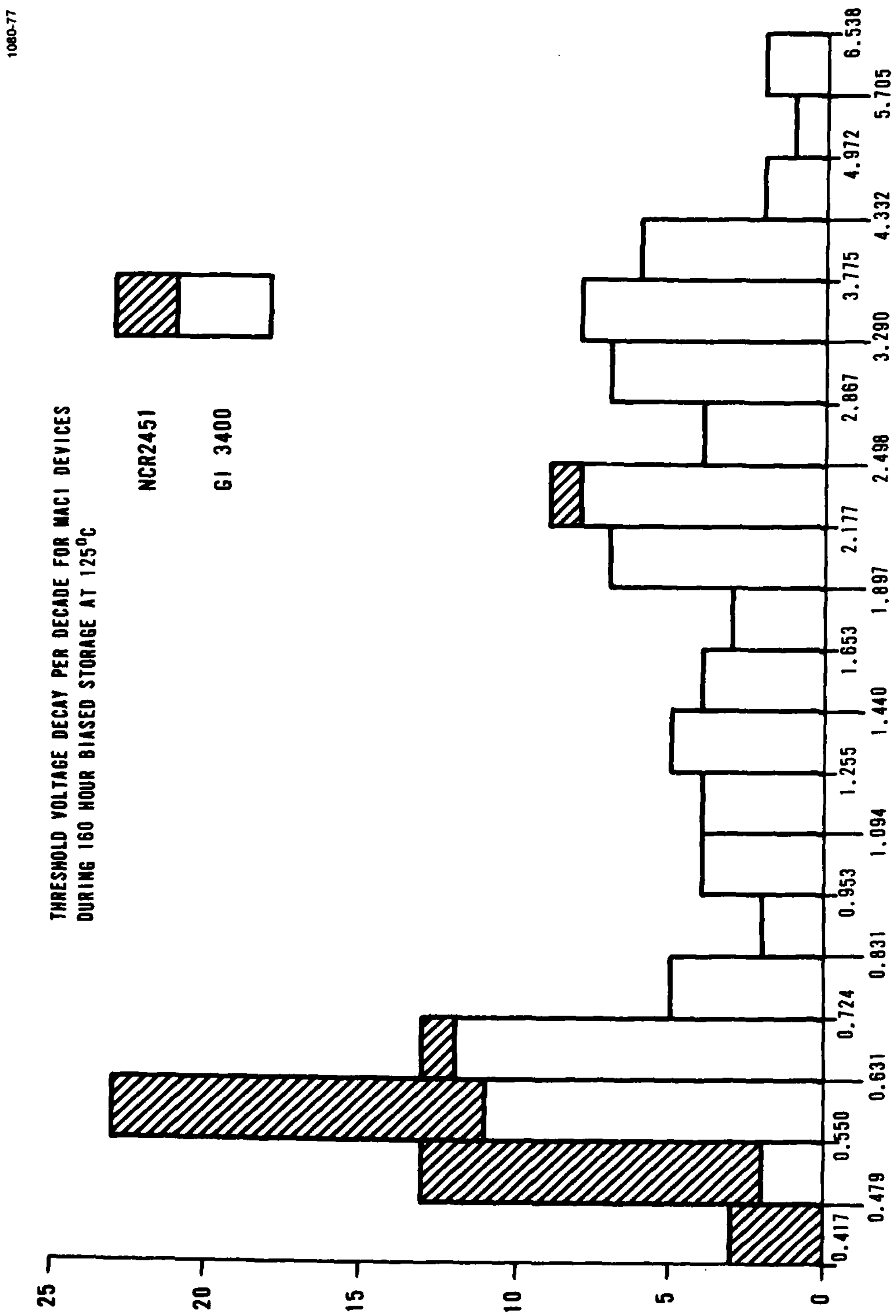


FIGURE 6-2. DISTRIBUTION OF RETENTION SLOPE (DISCHARGE RATE) FOR INITIAL MEASUREMENTS AT =125°C (NCR 2451/ER3400)

As indicated in Figure 6-1, four devices were lost in dc parameter tests. The third Interim Report, Section 7, covers the distributions of the measured dc parameter tests in detail. The dc parameter causing the most loss of devices was the VOL output voltage measurement at +125°C.

Other measurements, not part of the dc parameter testing but of interest to users, are the reference voltage and sense amp sensitivity measurements. The reference voltage is an internally generated voltage against which the threshold voltage is compared and thus determines the end of retention point for the retention curves.

Figure 6-3 shows the reference voltages of all ER3400 and NCR2451 devices tested. The sensitivity of the sense amp in comparing the threshold voltage to the reference voltage is measured by how close to the reference voltage the threshold is when the output sense changes. This is shown for all devices in Figure 6-4.

The final test was the functional after burn-in which eliminated five parts. These parts failed as a result of the effects of the 160 hour burn-in.

7. ACCELERATED TESTING OF TIME RELATED PARAMETER IN MNOS MEMORIES

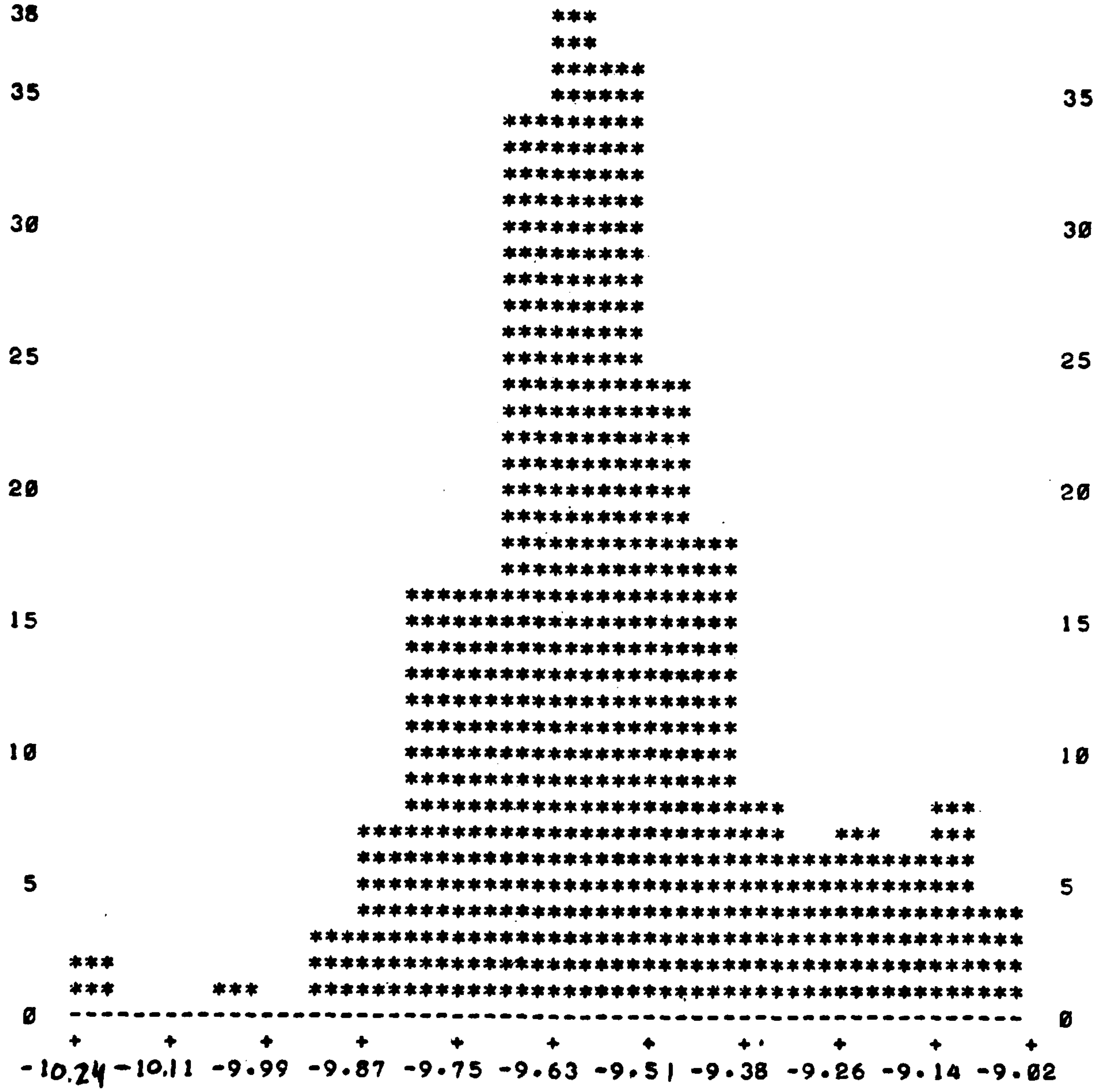
This very important section of the Third Interim Report discusses the development of accelerated and predictive tests used to screen MNOS devices for time related parameters previously measured on a lot sample basis. The correlation of the predictive methods is shown to be good for retention and endurance while the results for read-disturb retention prediction were inconclusive and require more testing and refinement.

Equations developed in the text of Section 8 of this report show retention time to be (using two threshold measurements).

Tr = retention time

$$Tr = \log^{-1}\left[\frac{(y-y_2)\ \lg \dfrac{T_2}{T_1}}{y_2-y_1} + \lg T_2\right]$$

234	NUMBER OF MEASUREMENTS
-9.54696581	MEAN
.197987368	ONE STANDARD DEVIATION
-10.24	MINIMUNVALUE
-9.02	MAXIMUM VALUE



REFERENCE VOLTAGE OF ALL TESTED MACI WAROMS
IN UNITS OF VOLTS

FIGURE 6-3. REFERENCE VOLTAGE OF ALL TESTED MACI WAROMS IN UNITS OF VOLTS

233	NUMBER OF MEASUREMENTS
.243733905	MEAN
.0659448202	ONE STANDARD DEVIATION
-.03	MINIMUNVALUE
.59	MAXIMUM VALUE

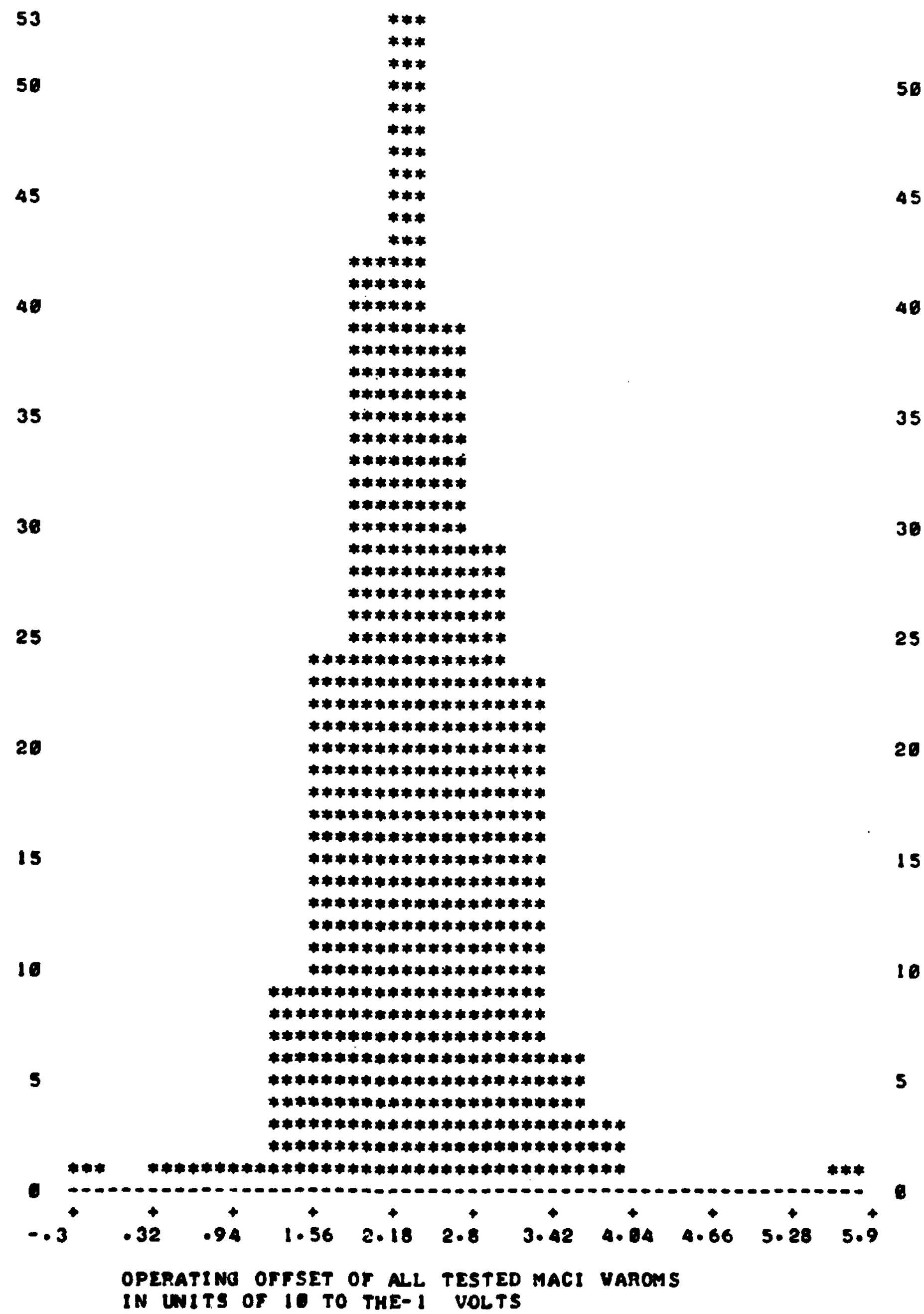


FIGURE 6-4. SENSE AMP SENSITIVITY

where

y = device threshold at end of retention.

y_1 = first threshold.

y_2 = second threshold.

T_1 = time of first Vt measurement after write.

T_2 = time of second Vt measurement after write.

NOTE

Y is developed from reference voltage minus sensitivity offset.

Continuing further refinement, Figure 7-1 shows a nomograph developed for screening devices for retention. Using two measurement points at 10800 sec (3 hours) and 160 hours after writing, the use of this nomograph quickly develops whether a 1 year retention is predicted for the part under test. Examples of its use are shown in the Third Interim Report.

For endurance prediction, Figure 7-2 shows the relationship of the soft erase threshold (i.e., Vt after a "normal" write and low voltage shortened erase is performed) to the measured endurance of ER3400/NCR2451 devices. From this newer device, soft erase thresholds are projected onto a best fit curve and their endurance characteristic after 10^5 E/W cycles predicted.

Nitride thickness was also related to erase substrate leakage and the correlation between leakage values taken during dc parameter testing and soft erase values was shown. This, then, directly relates the endurance to a leakage measurement test normally performed during screening with the potential for decreasing test time and cost to users seeking an efficient endurance screening method.

Investigations into the relationship between write speed and read disturb showed some promise, but due to the long time periods and tie-up of equipment and personnel, insufficient data was developed to show sufficient correlation or refine the method.

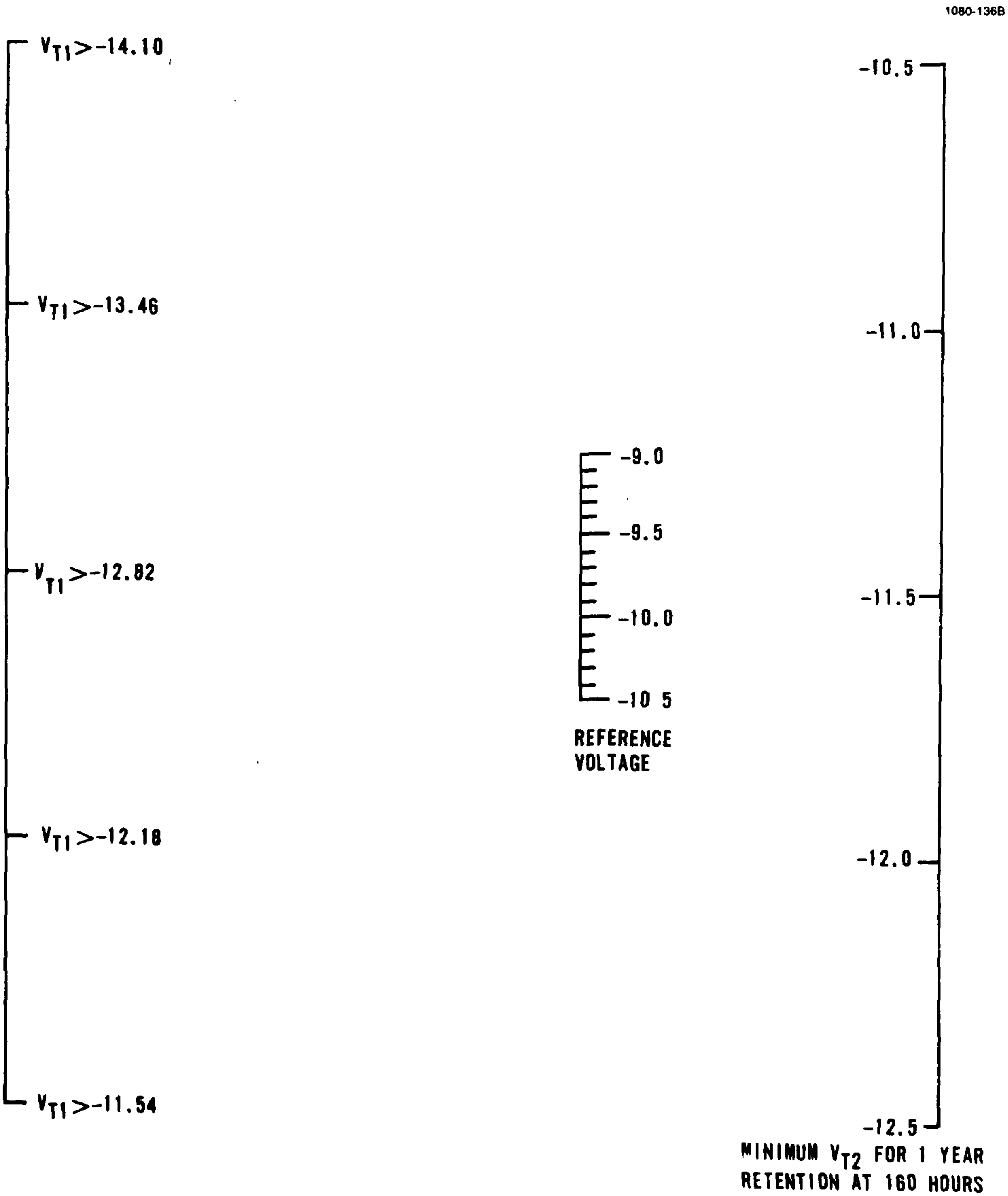


FIGURE 7-1. RETENTION NOMOGRAPH

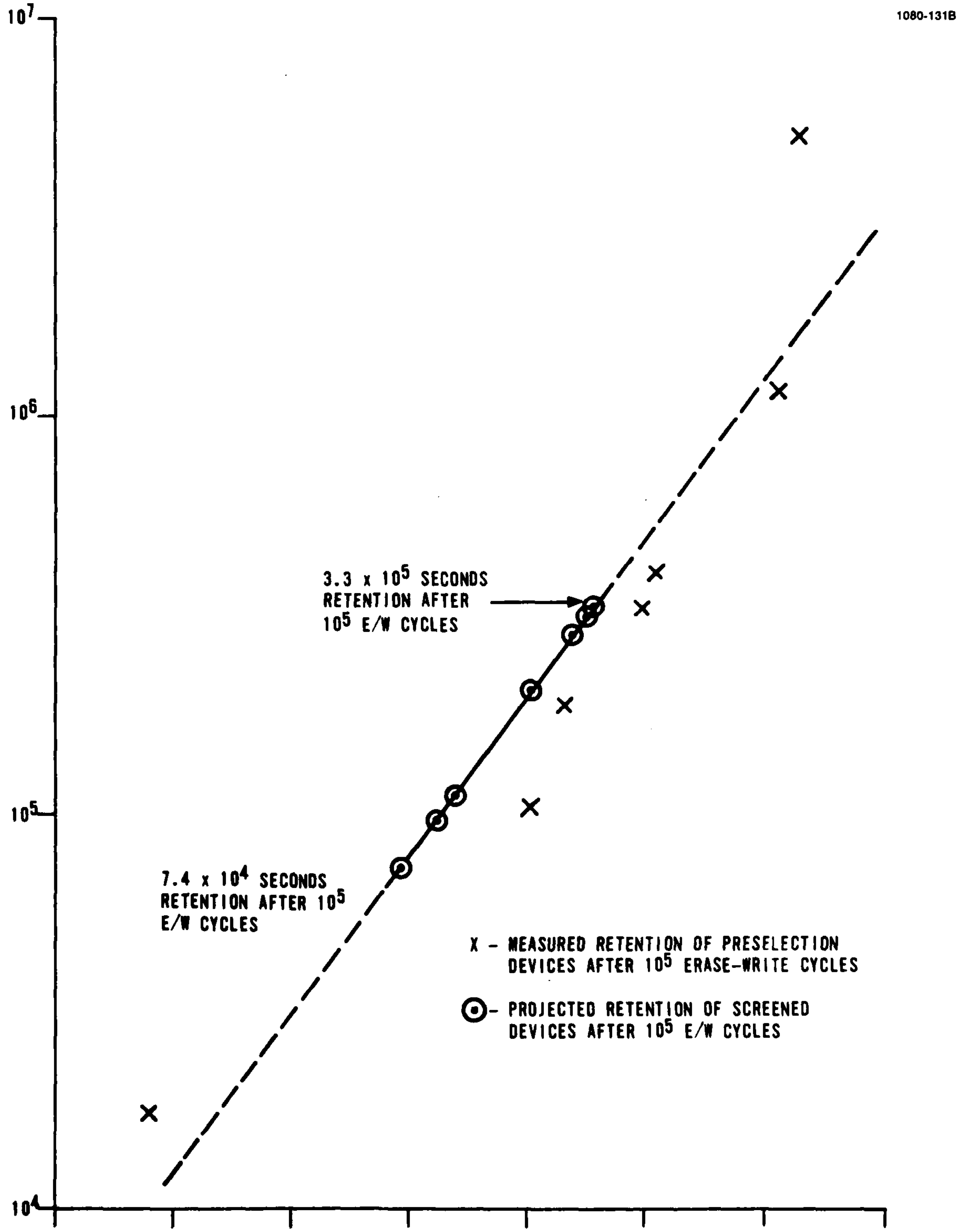


FIGURE 7-2. ENDURANCE VERSUS SOFT ERASE THRESHOLD

7.1 Conclusions

It was concluded that:

- Useful test methods were developed to ease the dilemma of users trying to perform cost effective screening of MNOS parts.
- Increased definition was brought to the MNOS industry by MACI to allow users insight into the pitfalls and benefits of MNOS device use.

8. PROPOSED SLASH SHEET

The complete final proposed slash sheet for NCR2451/ER3400 devices has been submitted to the contracting agency.

9. NEW TEST DATA

Table 8-1 shows radiation tests taken on ER3400 devices using a linac machine and varying the width and position of the radiation pulse with respect to the device read cycle. The upset levels shown had no data loss from radiation causes. The device losing data in the final test was traced to voltage sequencing problems during test.

New radiation testing performed on NCR2810/ER2810 devices showed that the ER2810 survived 50K rads (Si) of total dose with one of three surviving 100K rads TD. None of the NCR2810's reached 50K rads. All failures were traced to peripheral circuits and sense amps and did not represent memory transistor data loss.

10. DEVICE STATUS

The device status remains the same as for the Third Interim Report except that samples of Hitachi 48016 16K MNOS EAROM are now available and early preliminary testing indicates that a reasonable yield to military ranges may result. These devices represent next generation N Channel MNOS and are dense (16K bits) and fast (300 ns max = Tacc).

11. RECOMMENDED FUTURE STUDY

As a result of information learned from this MACI program, the following recommendations are made:

- After slash sheet approval it is recommended to urge vendors to place the NCR2451/ER3400 on QPL lists.

TABLE 8-1. ER3400 RADIATION TESTS

Device Type = ER 3400

UPSET LEVELS

Dev	Linac Pulse Width	Position/CE Pulse	Upset Level	Mode
		CE = 3.5 μs	rad(Si)/sec	
4	2.0 μs	0.5 μs before	5.4×10^6	RD
1	2.0 μs	0.5 & 2.5 μs after	5.4×10^6	RD
2	4.5 μs	0.5 μs before	5.4×10^6	RD

DATA RETENTION (No Data Loss)

Dev	Linac Pulse Width	Position/CE Pulse	Test Level	Mode
4	2 μs	1.0 μs before	5×10^8	RD
		2.0 μs after		

TOTAL DOSE

Dev	Linac Dose	Results	Mode
8	25K rads(Si)	No data loss	RD
8	40K rads	1 dev had some altered data	

- Development of a slash sheet for the NCR/GI 2810 8K EAROM is suggested which could be readily patterned after the proposed ER3400/NCR2451 slash sheet from the MACI program.

- New MACI Programs on next generation MNOS memories becoming available is highly recommended to allow defense contractors and military personnel insight into the test and application methods most suitable to these parts and to establish most promising candidates.

- Data developed under this program should be verified and kept current by potential users of these devices to allow for circuit and process changes that may result in the future.

12. CONCLUSIONS

- The MACI program has developed new testing methods that will be of great value to defense contractors and military personnel in applying MNOS devices.

- Due to ERADCOM's foresight into the true market conditions of semiconductor memories, devices that are extremely useful and cost effective in military applications can be used in a broad range of defense applications that will save significant funds and improve system performance.

- MACI-EAROM demonstrated that a complex technology can be tackled by this type program and produce useful results beneficial to both the military and industry.

- MACI-EAROM allows defense contractors not familiar with MNOS technology a "cookbook" type approach to teach them to become at least conversant with the technology and points out some of the pitfalls and opportunities presented by it.

- A proposed slash sheet for ER3400/NCR2451 devices to become QPL parts was developed.

DATE

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